Comparator

PIC 12F675

Zdeněk Matěj
72963@mail.muni.cz

Comparator

- The PIC12F629/675 devices have one analog comparator
- Compare two analog values

- On GP0 and GP1 are inputs to the comparator
- GP2 can be the comparator output
- Generates interrupt (CMIF)

Comparator - CMCON

REGISTER 6-1: CMCON — COMPARATOR CONTROL REGISTER (ADDRESS: 19h)

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0
bit 7							bit 0

bit 7 **Unimplemented**: Read as '0'

bit 6 **COUT**: Comparator Output bit
When CINV = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CINV = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 5 **Unimplemented**: Read as '0'

bit 4 **CINV**: Comparator Output Inversion bit
1 = Output inverted
0 = Output not inverted

bit 3 **CIS**: Comparator Input Switch bit
When CM2:CM0 = 110 or 101:
1 = VIN- connects to CIN+
0 = VIN- connects to CIN-

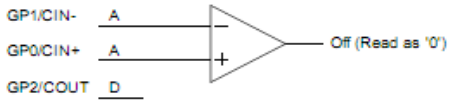
bit 2-0 **CM2:CM0**: Comparator Mode bits
Figure 6-2 shows the Comparator modes and CM2:CM0 bit settings

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

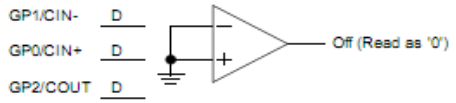
Comparator – operation modes

FIGURE 6-2: COMPARATOR I/O OPERATING MODES

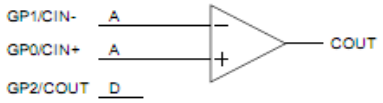
Comparator Reset (POR Default Value - low power)
CM2:CM0 = 000



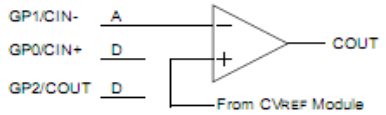
Comparator Off (Lowest power)
CM2:CM0 = 111



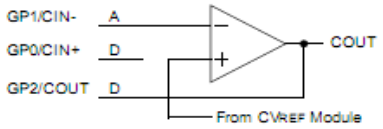
Comparator without Output
CM2:CM0 = 010



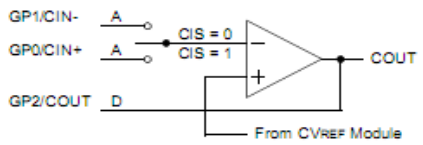
Comparator w/o Output and with Internal Reference
CM2:CM0 = 100



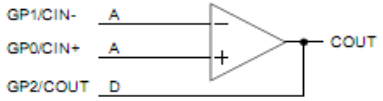
Comparator with Output and Internal Reference
CM2:CM0 = 011



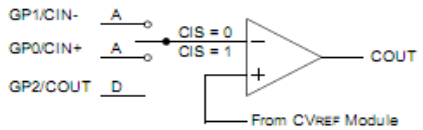
Multiplexed Input with Internal Reference and Output
CM2:CM0 = 101



Comparator with Output
CM2:CM0 = 001



Multiplexed Input with Internal Reference
CM2:CM0 = 110

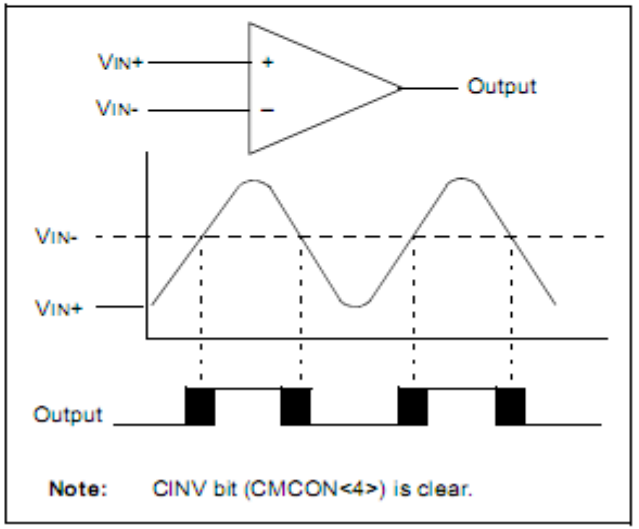


A = Analog Input, ports always reads '0'
D = Digital Input
CIS = Comparator Input Switch (CMCON<3>)

TABLE 6-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	COUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

FIGURE 6-1: SINGLE COMPARATOR



Note: CINV bit (CMCON<4>) is clear.

Comparator – voltage reference

- The voltage reference can output 32 distinct voltage levels

REGISTER 6-2: VRCON — VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 99h)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

bit 7 **VREN:** CV_{REF} Enable bit
1 = CV_{REF} circuit powered on
0 = CV_{REF} circuit powered down, no I_{DD} drain

bit 6 **Unimplemented:** Read as '0'

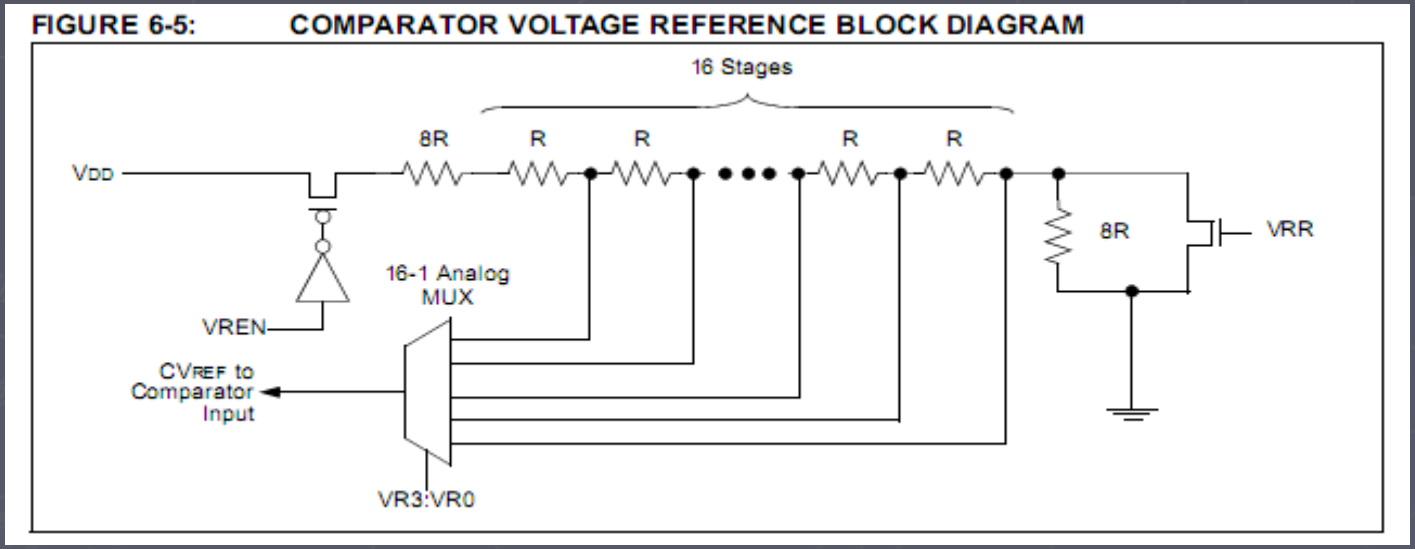
bit 5 **VRR:** CV_{REF} Range Selection bit
1 = Low range
0 = High range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR3:VR0:** CV_{REF} value selection $0 \le VR[3:0] \le 15$
When VRR = 1: $CV_{REF} = (VR3:VR0 / 24) * V_{DD}$
When VRR = 0: $CV_{REF} = V_{DD}/4 + (VR3:VR0 / 32) * V_{DD}$

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Comparator – voltage reference



Comparator - example

```
//init
// - COUT - CINV CIS CM2 CM1 CM0
CMCON=0;

output=COUT;
```

References

Source:
http://ww1.microchip.com/downloads/en/devicedoc/41190c.pdf