PIC12F629 / 675
EEPROM

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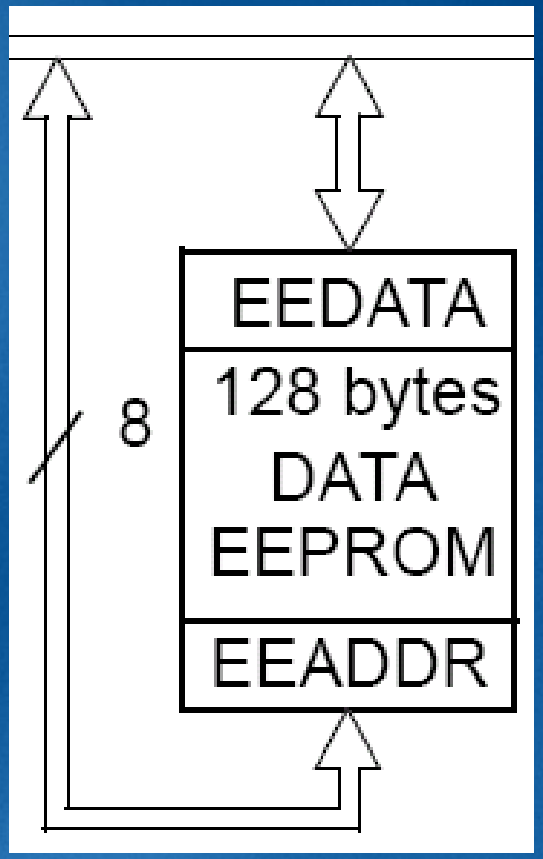
Package

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	FLASH (words)	SRAM (bytes)	EEPROM (bytes)				
PIC12F629	1024	64	128	6	–	1	1/1
PIC12F675	1024	64	128	6	4	1	1/1



EEPROM - Basics

- Readable and writable during normal voltage,
- memory is not directly accessible, it's mapped in the register file space,
- there are four control registers:
  - EECON1, EECON2, EEDATA, EEADR
- address range from 0h to 7Fh
- interrupt on write complete (EEIF)

Registers Eeprom

REGISTER 8-1: EEDAT — EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

bit 7-0 **EEDATn**: Byte value to write to or read from Data EEPROM

REGISTER 8-2: EEADR — EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
bit 7							bit 0

bit 7 **Unimplemented**: Should be set to '0'

bit 6-0 **EEADR**: Specifies one of 128 locations for EEPROM Read/Write Operation

Registers Eeprom (cont.)

REGISTER 8-3: EECON1 — EEPROM CONTROL REGISTER (ADDRESS: 9Ch)

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit

1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOD detect)

0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit

1 = Allows write cycles

0 = Inhibits write to the data EEPROM

bit 1 **WR**: Write Control bit

1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)

0 = Write cycle to the data EEPROM is complete

bit 0 **RD**: Read Control bit

1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software).

0 = Does not initiate an EEPROM read

Read sequence

```
bsf     STATUS,RP0    ;Bank 1
movlw   ADDRESS       ;
movwf   EEADR         ;Address to read
bsf     EECON1,RD     ;EE Read
movf    EEDATA,W      ;Move data to W
```

Write sequence

```
bsf             STATUS,RP0   ;Bank 1
movlw           <value>
movwf           EEDATA                  ; Data to write
movlw           <address>
movwf           EEADR                   ; Address to write
bsf             EECON1,WREN ; Enable write
bcf             INTCON,GIE              ; Disable INTs
movlw           0x55                    ; Unlock write
movwf           EECON2                  ;
movlw           0xAA                    ;
movwf           EECON2                  ;
bsf             EECON1,WR               ; Start the write
Loop:
        btfsc           EECON1,WR       ; Waiting until
        goto            Loop            ; write is finished
bsf             INTCON,GIE              ; Enable INTS
```

Verify sequence

```
bcf       STATUS,RP0    ;Bank 0
:                       ;Any code
bsf       STATUS,RP0    ;Bank 1 READ
movf      EEDATA,W      ;EEDATA not
     changed from previous write
bsf       EECON1,RD     ;<Y>, Read the
                        ;value written
xorwf     EEDATA,W
btfss     STATUS,Z      ;Is data the same
goto      WRITE_ERR     ;<N> handle error
:                       ;<Y>, continue
```

EEPROM Registers

TABLE 8-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
9Ah	EEDATA	EEPROM Data Register								0000 0000	0000 0000
9Bh	EEADR	—	EEPROM Address Register							-000 0000	-000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2(1)	EEPROM Control Register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by Data EEPROM module.

Note 1: EECON2 is not a physical register.