Microcontrollers

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Microcontroller

...also referred to as: MCU, uC, μC.

- MCU is basically a "computer-on-a-chip": microprocessor, data and program memory, I/O peripherals; usually also interrupt controller, timers, non-volatile storage (EEPROM)
- Various extra peripherals usually integrated : analog peripherals (A/D, D/A, comparators), serial communication (UART, SPI, IIC), drivers (LCD, PWM)
- Typically used for low-cost, space- and power-critical applications
- Simple architecture also allows for better real-time capabilities.

Special branch of MCUs targeted at signal processing is recognized as the Digital Signal Controllers, DSCs.

Scale

- Data memory: from 16B to several MB
- Program memory: from 250 words to several MB
- Clock speed: typically a few MHz (1-20), 32kHz for ultra low power, 500+ for hi-end cores
- I/O size: from 6 pins (incl. power)

μC vs. microprocessor

- all components on a single chip
- fixed memory and I/O size
- for cost / power / space -critical applications
- reduced complexity $\Rightarrow$ reliability, real-time response

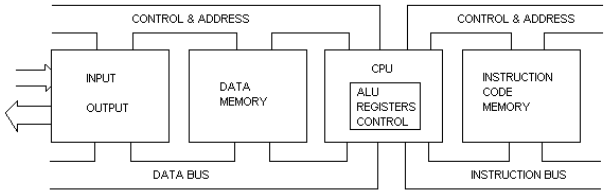
- only processing unit, the rest connected externally
- modularity: arbitrary I/O and memory
- performance
- versatile, expandable

Nowadays both can be either general purpose or application specific.

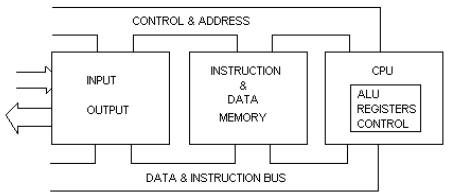
MCU Taxonomy

- architecture: Von Neumann, (Modified) Harvard
- instruction set: RISC, CISC, ...
- addres bus width: 8-, 16-, 32-, 64-bit
- platform: IC, soft-core
- family: acording to manufacturer (see [1])

Harvard vs. von Neumann



HARVARD ARCHITECTURE MICROPROCESSOR



VON NEUMANN ARCHITECTURE MICROPROCESSOR

In Von Neumann architecture, the data and program memory are stored in a single memory $\Rightarrow$ more universal concept

In Harvard architecture, there are separate memories and buses for data and program memory $\Rightarrow$ simultaneous access to instructions and data, different bus widths.

Basic models developed

Modified Harvard architecture: the architecture allows for modification of the program memory from the system itself, e.g by special instructions

Memory mapped I/O: the peripheral interfaces are mapped into single continguous memory space.

Instruction sets

Complete Instruction Set Computer (CISC): large instruction set performing even complex tasks; usually takes several clock cycles to execute – e.g. Intel 80x86, Zilog Z80, 8051

Reduced Instruction Set Computer (RISC): small instruction set, fast and fixed time execution (good for pipelining); complex task are done as a combination of more instructions – e.g. ARM, Sparc, Atmel AVR MIPS, PowerPc, PIC

Today, an amorphous combination is typically used, the only CISC computers are x86s.

Introducing PICs

PIC ... Peripheral Interface Controller or Programable Intelligent Controller by Microchip company

Popular for wide range of devices with uniform design concepts, low cost devices, free or low cost development tools, serially reprogrammable instruction memory, large user base, extensive collection of application notes and support materials.

PIC families

- 8-bit controllers: PIC10, PIC12, PIC16, PIC18
- 16-bit general purpose: PIC24F, PIC24H/E
- 16-bit digital signal controllers: dsPIC30, dsPIC33
- 32-bit controllers: PIC32

General properties

- Modified Harvard architecture – separate code and data space
- RISC – small amount of fixed-length instructions
- single cycle instruction execution (1-4 clock cycles)
- small adressable data space, extended through banking
- memory-mapped registers & peripherals (all in single address space)
- low power consumption: scalable oscillators, power-down modes, peripherals disabling
- hardware stack (8-bits)

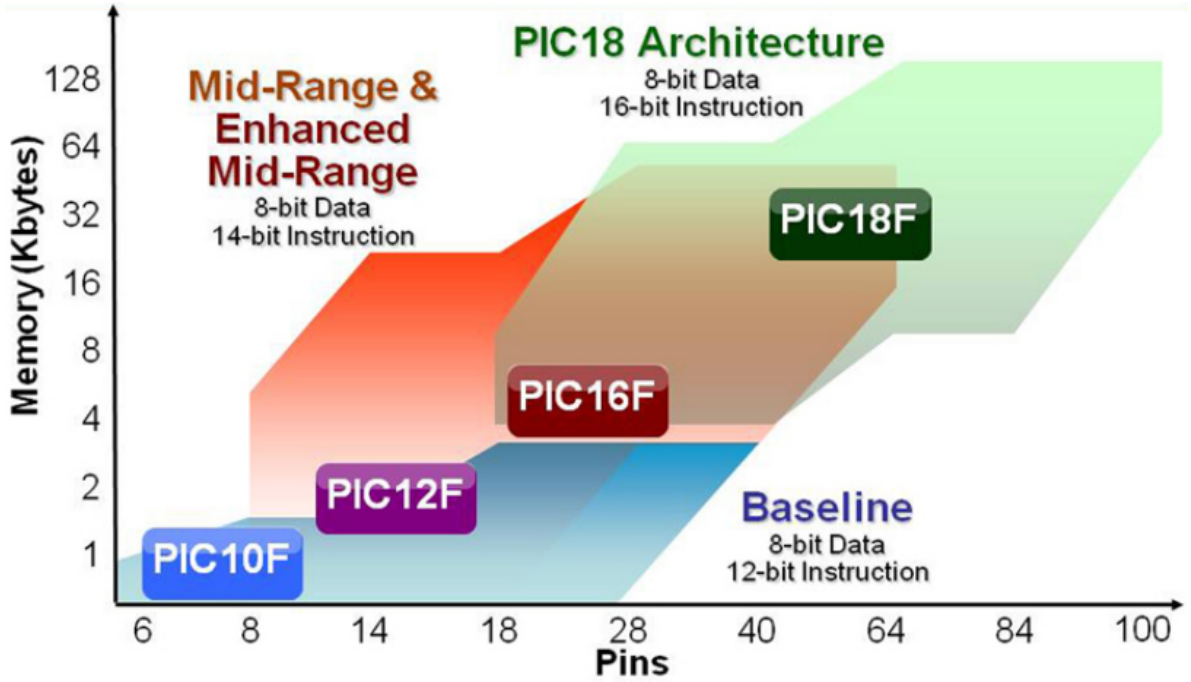
Typical features

- General purpose I/O pins
- Internal clock oscillators
- 8/16/32-bit timers
- Watchdog timer with separate clock oscillator.
- Internal non-volatile memory (EEPROM)
- ICSP – in-circuit serial programming

Typical features II.

- Synchronous/Asynchronous Serial Interface USART.
- MSSP Peripheral for I^2C and SPI Communications.
- Capture/Compare and PWM modules
- Analog peripherals: A/D converters (up to 1.0 MHz), DAC, comparator, voltage references
- USB, Ethernet, CAN interfacing support.
- External memory interface.

8-bit Core Architectures

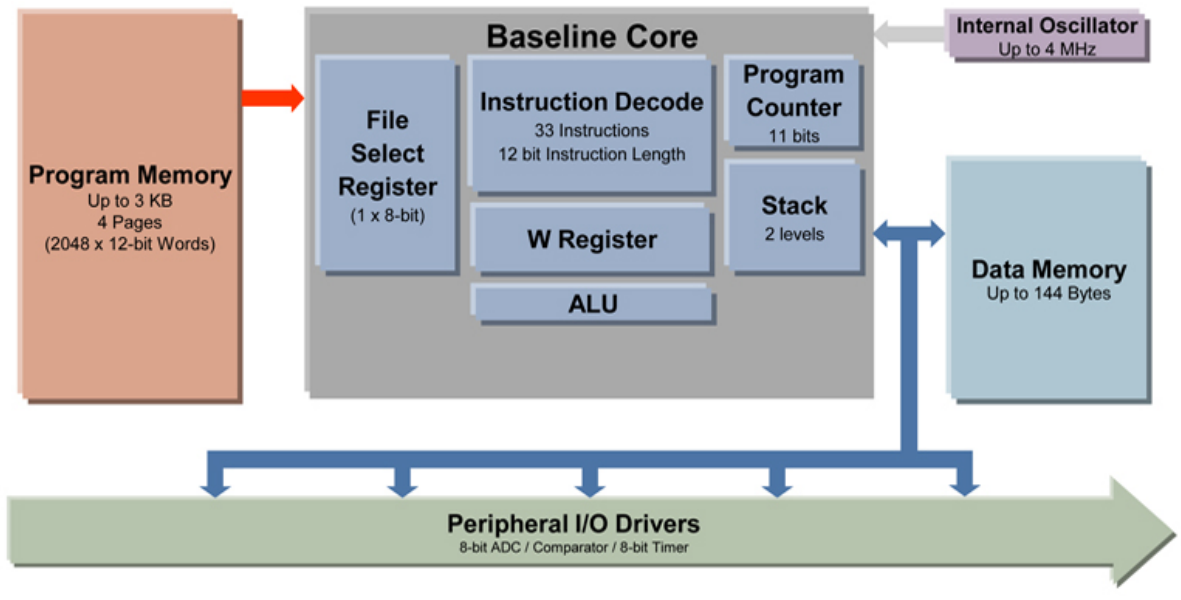


8-bit Families

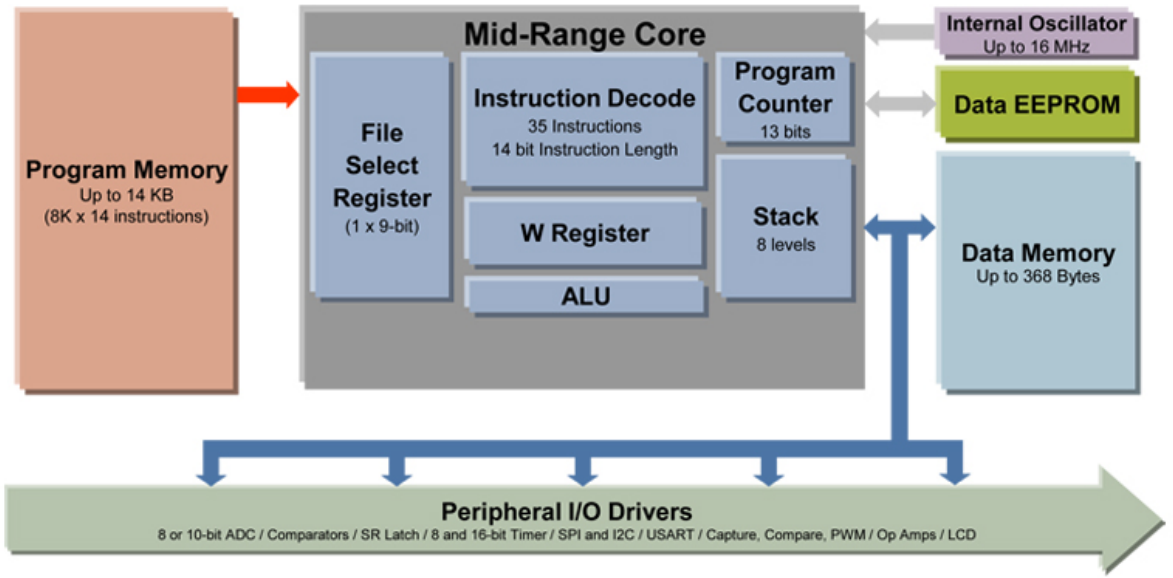
Compare 8-bit PIC® MCU Architectures

	Baseline Architecture	Mid-Range Architecture	Enhanced Mid-Range Architecture	PIC18 Architecture
Pin Count	6-40	8-64	8-64	18-100
Interrupts	No	Single interrupt capability	Single interrupt capability with hardware context save	Multiple interrupt capability with hardware context save
Performance	5 MIPS	5 MIPS	8 MIPS	Up to 16 MIPS
Instructions	33, 12-bit	35, 14-bit	49, 14-bit	83, 16-bit
Program Memory	Up to 3 KB	Up to 14 KB	Up to 28 KB	Up to 128 KB
Data Memory	Up to 138 Bytes	Up to 368 Bytes	Up to 1,5 KB	Up to 4 KB
Hardware Stack	2 level	8 level	16 level	32 level
Features	▪ Comparator ▪ 8-bit ADC ▪ Data Memory ▪ Internal Oscillator	In addition to Baseline: ▪ SPI/I²C™ ▪ UART ▪ PWMs ▪ LCD ▪ 10-bit ADC ▪ Op Amp	In addition to Mid-Range: ▪ Multiple Communication Peripherals ▪ Linear Programming Space ▪ PWMs with Independent Time Base	In addition to Enhanced Mid-Range: ▪ 8x8 Hardware Multiplier ▪ CAN ▪ CTMU ▪ USB ▪ Ethernet ▪ 12-bit ADC
Highlights	Lowest cost in the smallest form factor	Optimal cost to performance ratio	Cost effective with more performance and memory	High performance, optimized for C programming, advanced peripherals
Total Number of Devices	16	58	29	193
Families	PIC10, PIC12, PIC16	PIC12, PIC16	PIC12FXXX, PIC16F1XX	PIC18

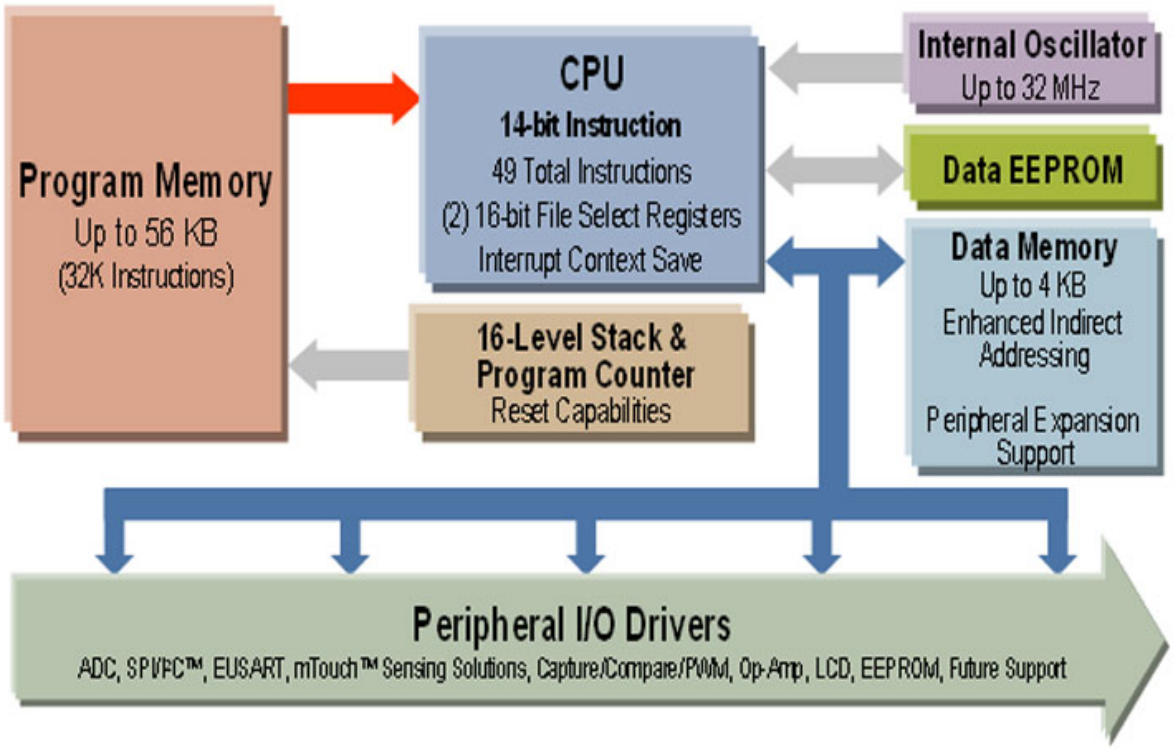
8-bit Baseline architecture



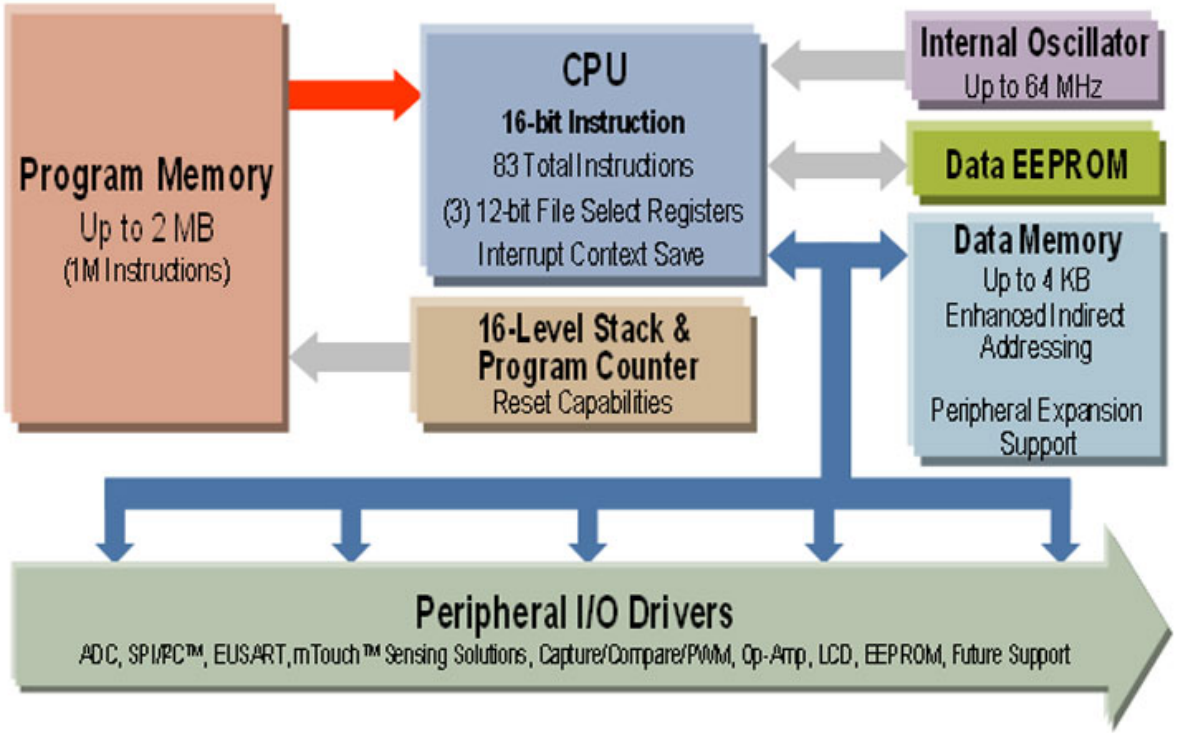
8-bit Mid-range architecture



8-bit Enhanced mid-range architecture



8-bit PIC18 architecture



16-bit Families

PIC24F: Low Power

- Low cost 16-bit families
- eXtreme Low Power (XLP) devices
- 16 MIPS performance @ 3.3V
- Up to 96 KB RAM
- Integrated USB-OTG, Graphics, CTMU and RTCC
- Motor Control Peripherals

PIC24H/E: Highest Performance

- Up to 70 MIPS performance at 3.3V
- High performance 10/12-bit ADC
- DMA channels for faster data transfer
- Motor Control peripherals and integrated op amps
- Up to 2 CAN, I²C™, SPI and PMP
- Extended and high-temperature(150°C) options

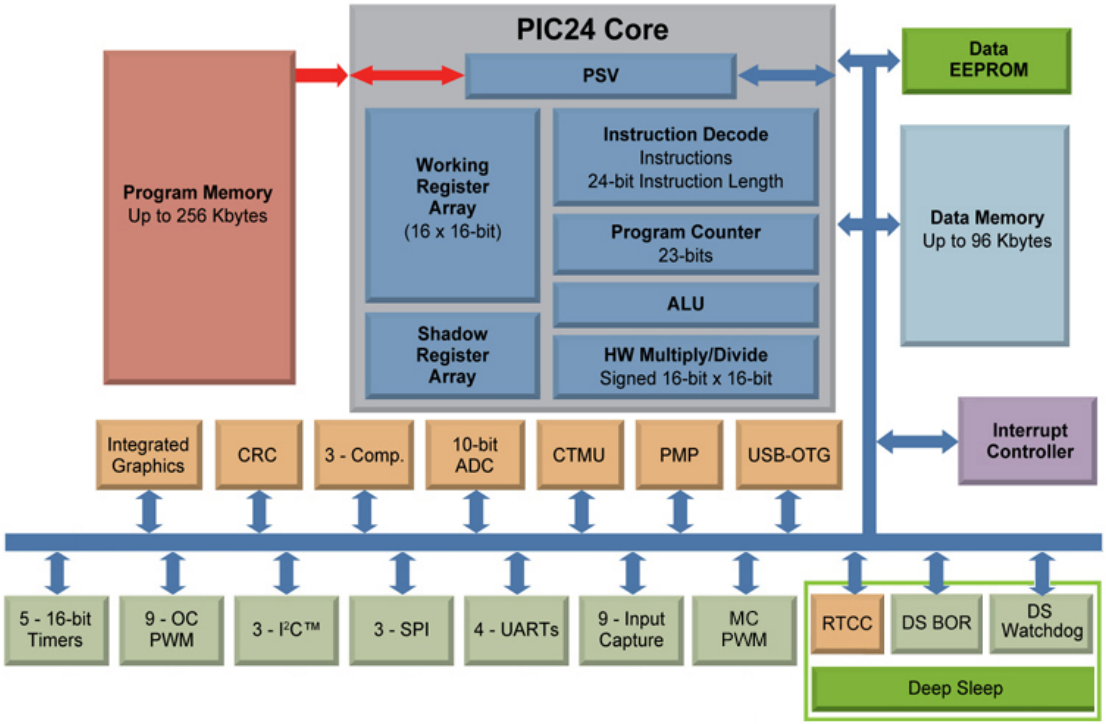
dsPIC30F: Versatile 5V DSCs

- 30 MIPS DSP performance 5V
- Up to 4 KB EEPROM
- Motor Control peripherals
- Integrated Codec interface

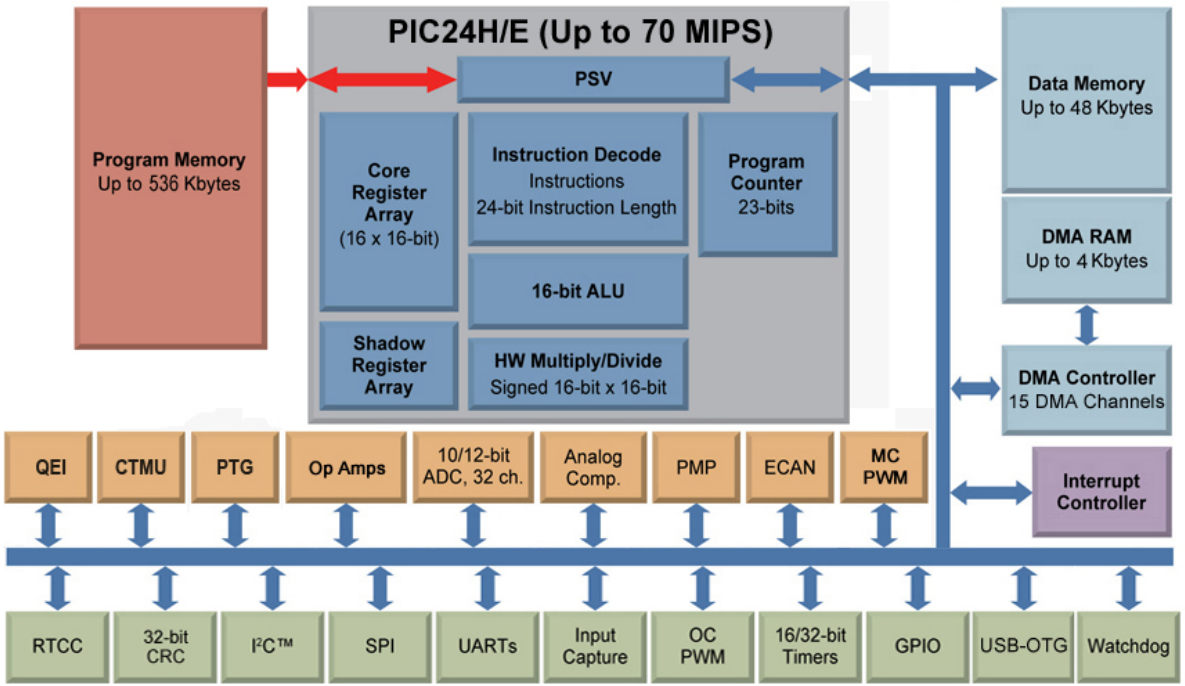
dsPIC33F/E: High Performance DSCs

- Up to 70 MIPS DSP performance at 3.3V
- Up to 32 Ch. high performance 10/12-bit ADCs
- Digital Power, Motor Control and Audio Peripherals
- Integrated Op Amps
- Up to 2 CAN, I²C™, SPI and PMP
- Extended and high-temperature(150°C) options

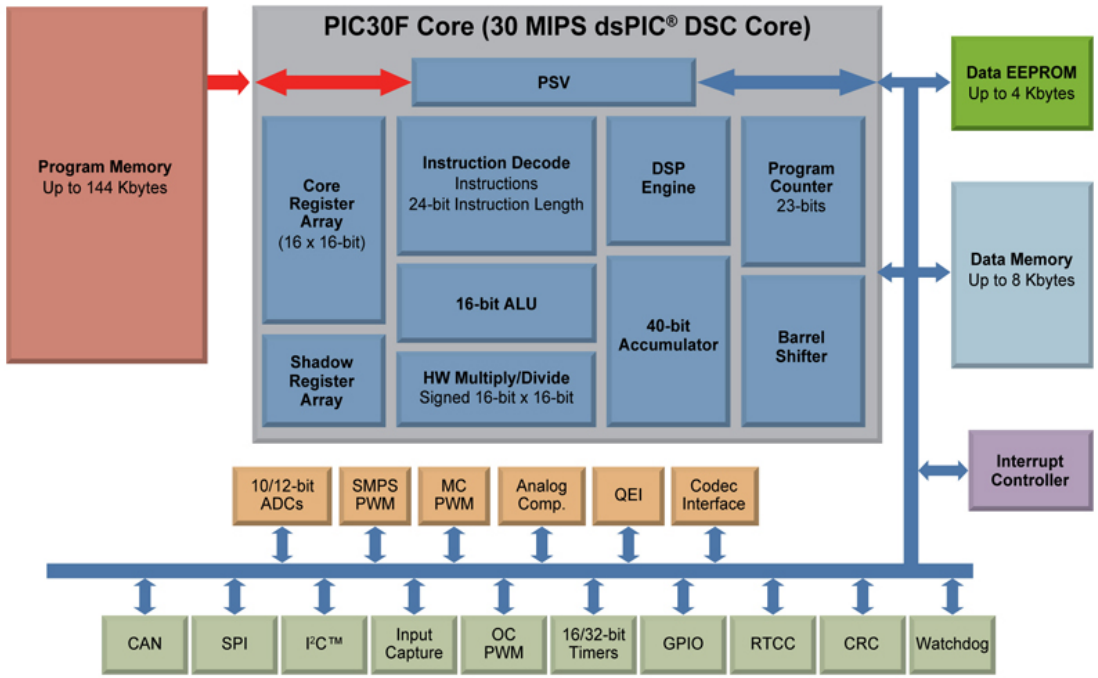
16-bit PIC24F architecture



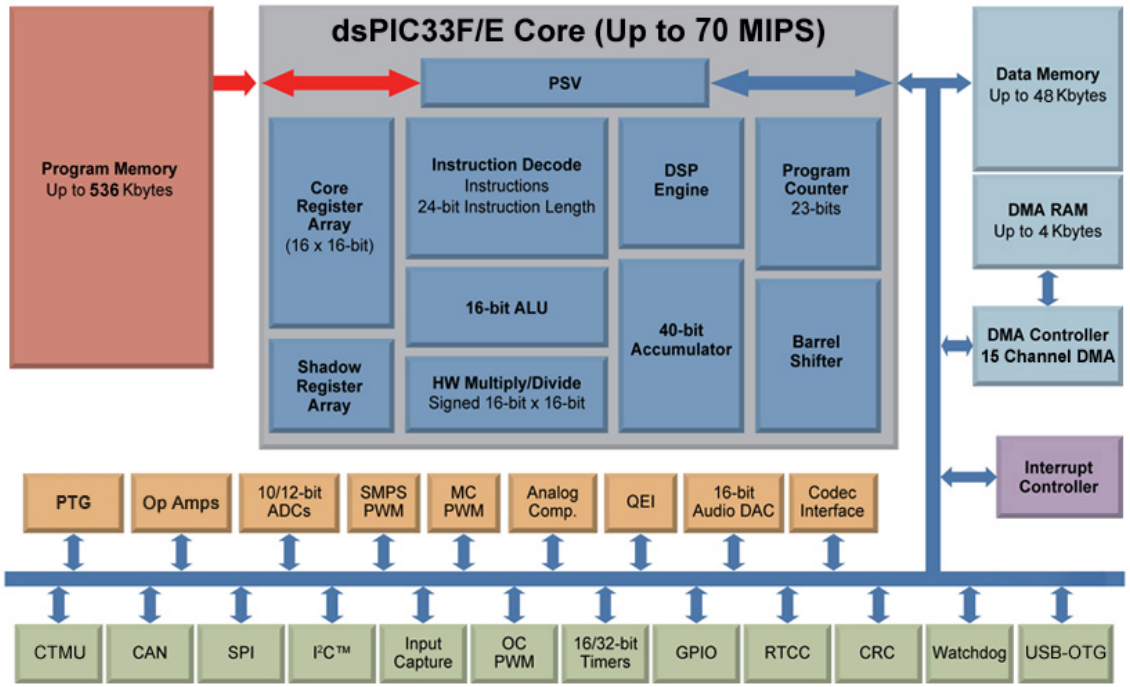
16-bit PIC24E/H architecture



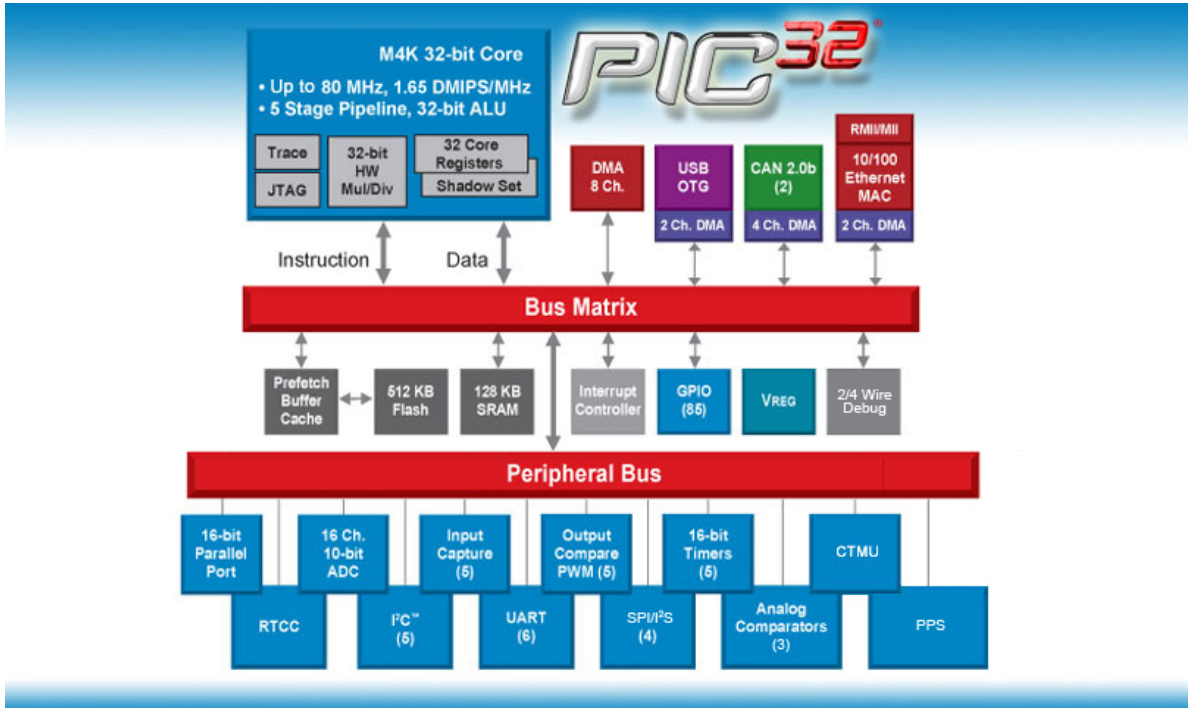
16-bit dsPIC30 architecture



16-bit dsPIC33 architecture



32-bit Family



References

[1] List of common microcontrollers

http://en.wikipedia.org/wiki/List_of_common_microcontrollers

[2] Microchip company website

http://www.microchip.com