PIC12F629 / 675
Using Watchdog

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Watchdog Timer

- provides recovery from a system problem
  - e.g. a program that goes into an endless loop, or a hardware problem that prevents the program from operating correctly
- if the program doesn't reset the watchdog at some predetermined interval, a hardware reset will be initiated
- useful for unattended systems
- running both in normal and sleep mode
  - normal mode – on overflow it initiates RESET
  - sleep mode – on overflow it initiates wake-up
- CLRWDT instruction resets the watchdog timer

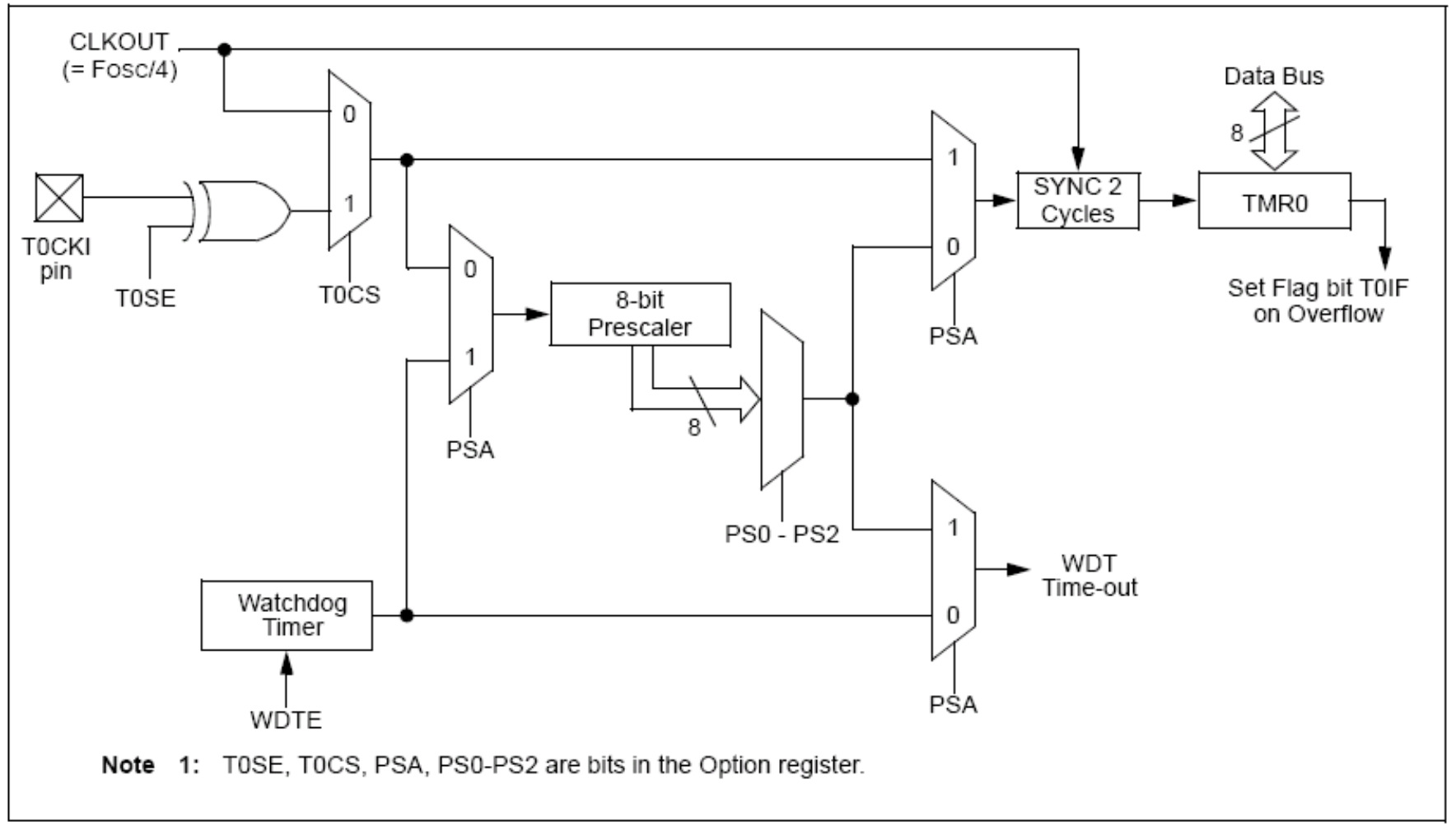
Watchdog period

- a nominal time-out period of 18 ms (with no prescaler)
- a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register
  - -> max. period 2,3s
  - CLRWDT and SLEEP instructions clear the timer AND prescaler

Watchdog Timer in C

- in the header we have to enable or disable watchdog by WDTEN or WDTDIS configuration bits:
  - `__CONFIG(MCLRDIS & WDTEN & INTIO);`
- CLRWDT() macro in C resets watchdog

Watchdog Block Diagram



Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the Option register.

Watchdog Registers

TABLE 9-9: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
81h	OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
2007h	Config. bits	$\overline{CP}$	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	F0SC2	F0SC1	F0SC0	uuuu uuuu	uuuu uuuu

Legend: u = Unchanged, shaded cells are not used by the Watchdog Timer.

Watchdog registers

REGISTER 2-2: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{GPPU}}$**: GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of GP2/INT pin
0 = Interrupt on falling edge of GP2/INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on GP2/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on GP2/T0CKI pin
0 = Increment on low-to-high transition on GP2/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the TIMER0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128