

PA221

Spring 2022

Organization

- Seminars
 - Mostly you working on various tasks
- Final project
- End of semester:
 - Hand in exercise solutions
 - Project + report (3-4 pages of text)

Verilog Simulation with Icarus Verilog

- Icarus Verilog
 - Compile Verilog into an executable.
 - Windows installers: <https://bleyer.org/icarus/>, let the installer update PATH
- GTKWave
 - For reading and displaying waveform files.
 - Windows build: <https://sourceforge.net/projects/gtkwave/files/>, find a recent file with the bin-win64.zip or bin-win32.zip suffix, unpack anywhere, the binary is in bin/gtkwave..

Verilog Simulation with Icarus Verilog: MWE

Create a text file hello.v with the following contents:

```
module hello;  
initial begin  
    $display("Hello world!\n");  
    $finish;  
end  
endmodule
```

Compile and run it with:

```
iverilog -o hello hello.v  
vvp hello
```

Verilog Simulation with Icarus Verilog: Example

Download and extract fixpkt.zip from the study materials.

Compile and run the testbench using:

```
iverilog -o fixpkt fixpkt.v fixpkt_tb.v  
vvp fixpkt
```

Examine the generated fixpkt_tb.vcd using GTKWave.

Verilog Simulation with Icarus Verilog: Task

Write your own testbench.

You can use delays (**#10**) anywhere, all kinds of loops, **initial** statements are fully supported, file I/O works.