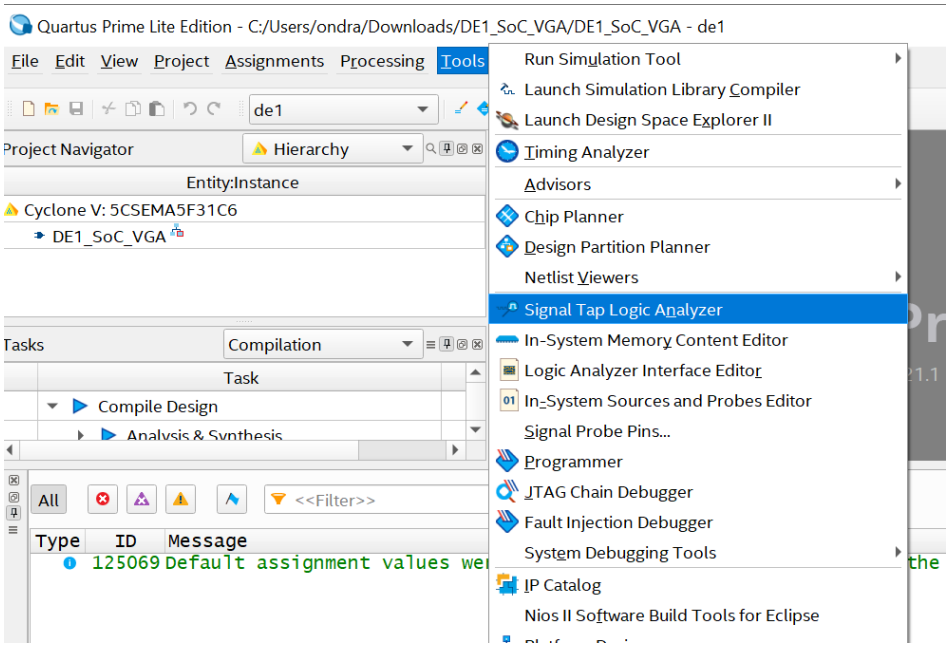
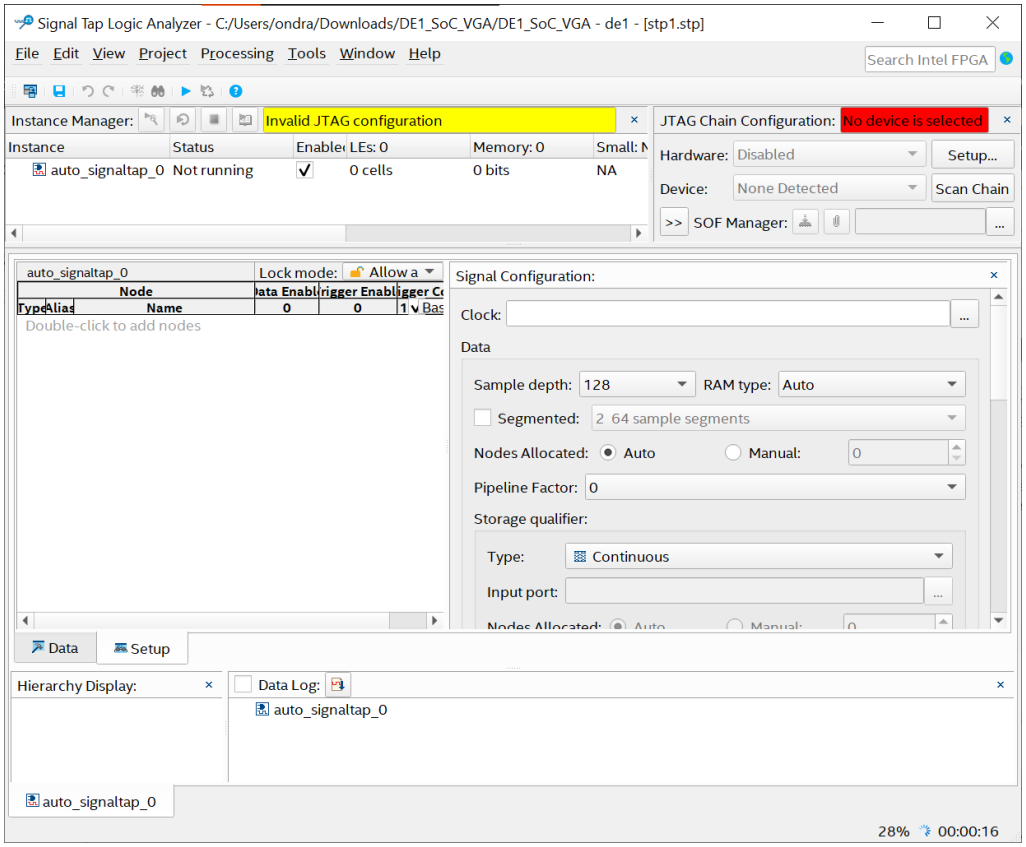
SignalTap Quickstart

Signal Tap allows you to inspect the signals inside a real FPGA by inserting a logic analyzer module into your design and interfacing with it using a GUI on your computer.

1. Open a project you want to inspect. If you don't have one, you can get **DE1_SoC_VGA** from the study materials.
2. Start SignalTap from the **Tools** menu in Quartus.

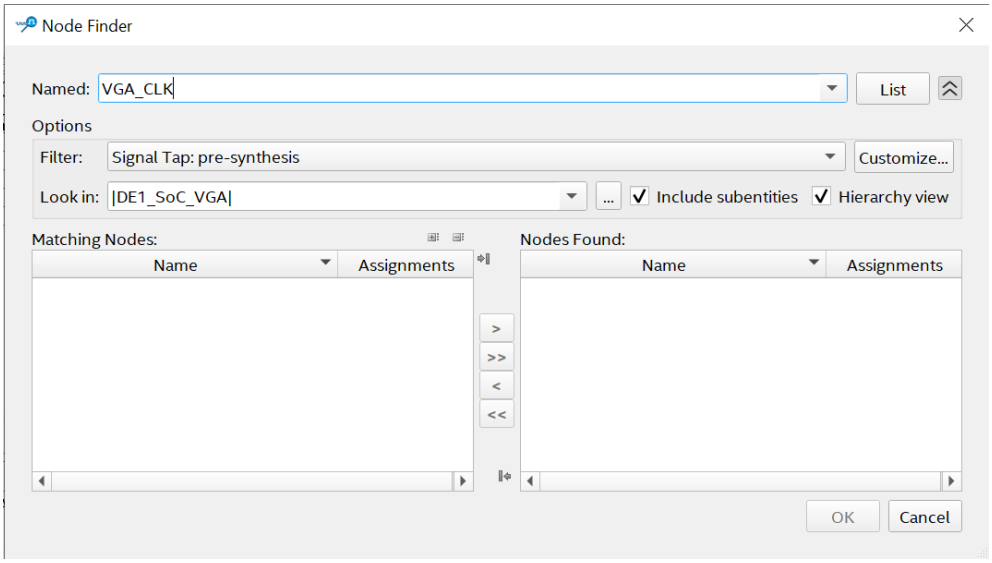


3. Signal Tap will open.

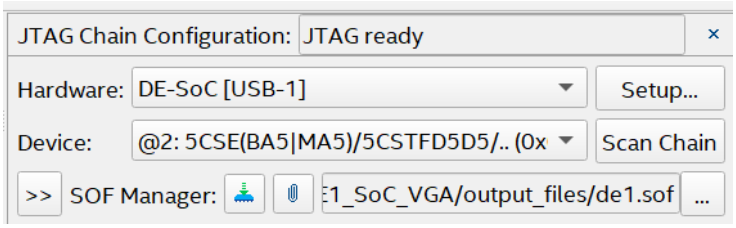


4. At this point, you won't be able to add any signals. For the signals to become available, run compilation in Quartus. Up to the **Place & Route** step is enough. When the compilation finishes, select your clock signal. Click the button with three dots in the **Signal Configuration** next to the **Clock** textbox to open a selection window. Enter an expression which describes your clock signal name. I chose the **VGA_CLK** signal. You can use wildcards for the search. The **Filter** dropdown allows you to find signals as interpreted in different stages of compilation. "Design Entry" is closest to what is written in the source code, but it might not be what the resulting design contains, so it might be more difficult for the tools to close timing or more expensive to recompile the design with

the probes inserted. Move the clock signal to the right column and click **OK**.

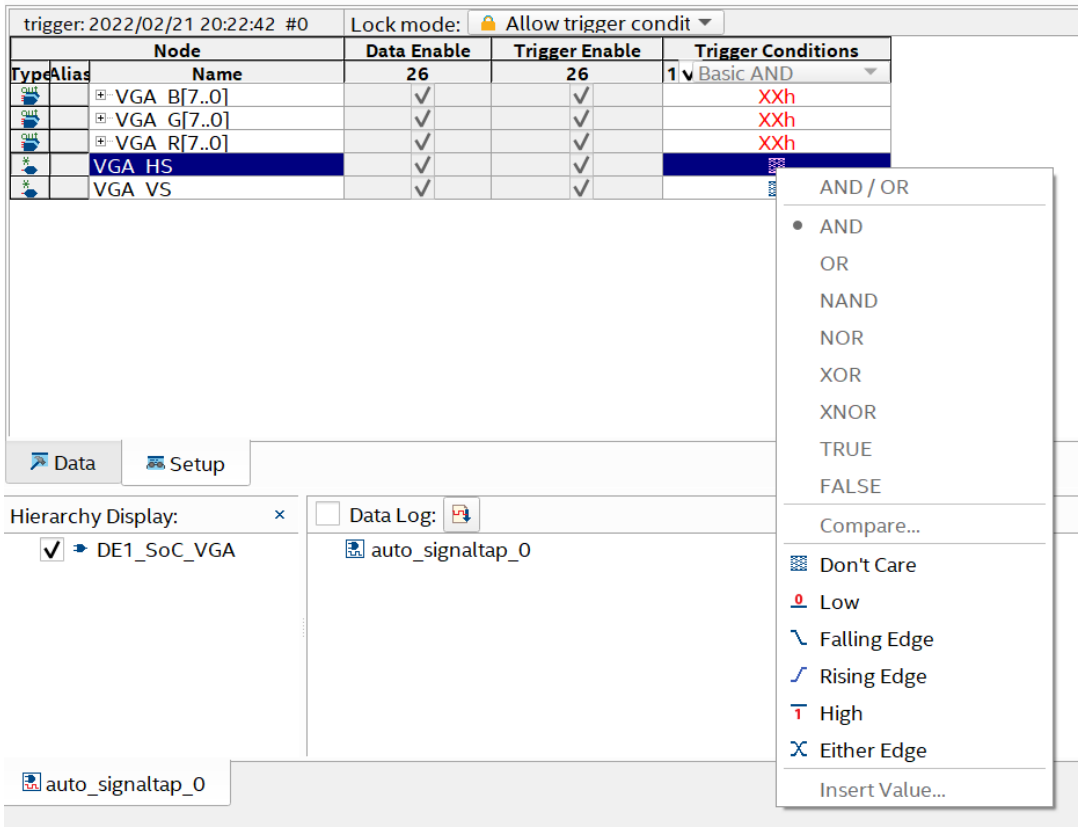


5. Now add the data signals you want to watch by double-clicking in the left pane of the main window. I selected **VGA_R**, **VGA_G**, **VGA_B**, **VGA_HS**, and **VGA_VS**.
6. You can now configure the capture parameters in the **Signal Configuration** pane. Important is the **Sample Depth** parameter. Higher values lets you see more context, but require more storage elements inside the FPGA.
7. Start the compilation by clicking the blue arrow in the top bar. Click **Yes** multiple times and wait for the compilation to finish.
8. Attach the FPGA using the BLASTER USB interface to the computer and power it up.
9. Configure the JTAG connection in the top-right pane: select the connection to your board in the **Hardware** dropdown, select the FPGA from the **Device** dropdown and load the **.sof** file generated during the compilation. The result should look like this:



10. Program the FPGA using the **Program device** button located next to the “SOF Manager:” label.
11. Now the design is running, but the logic analyzer is still idle. Start it using the **Run Analysis** or **Autorun Analysis** buttons. The first is one-shot, while the second retriggers automatically.
12. The data is now coming in.

13. To choose which data you want to see, change **trigger conditions** on the **Setup** pane:



When you are done with debugging, do not forget to get rid of the files the analyzer inserted into your project! It slows the compilation down considerably and uses valuable FPGA resources. In the Quartus project settings (**Assignments** -> **Settings**):

1. Disable Signal Tap on the **Signal Tap Logic Analyzer** pane.
2. Remove **.stp** files from the **Files** pane.