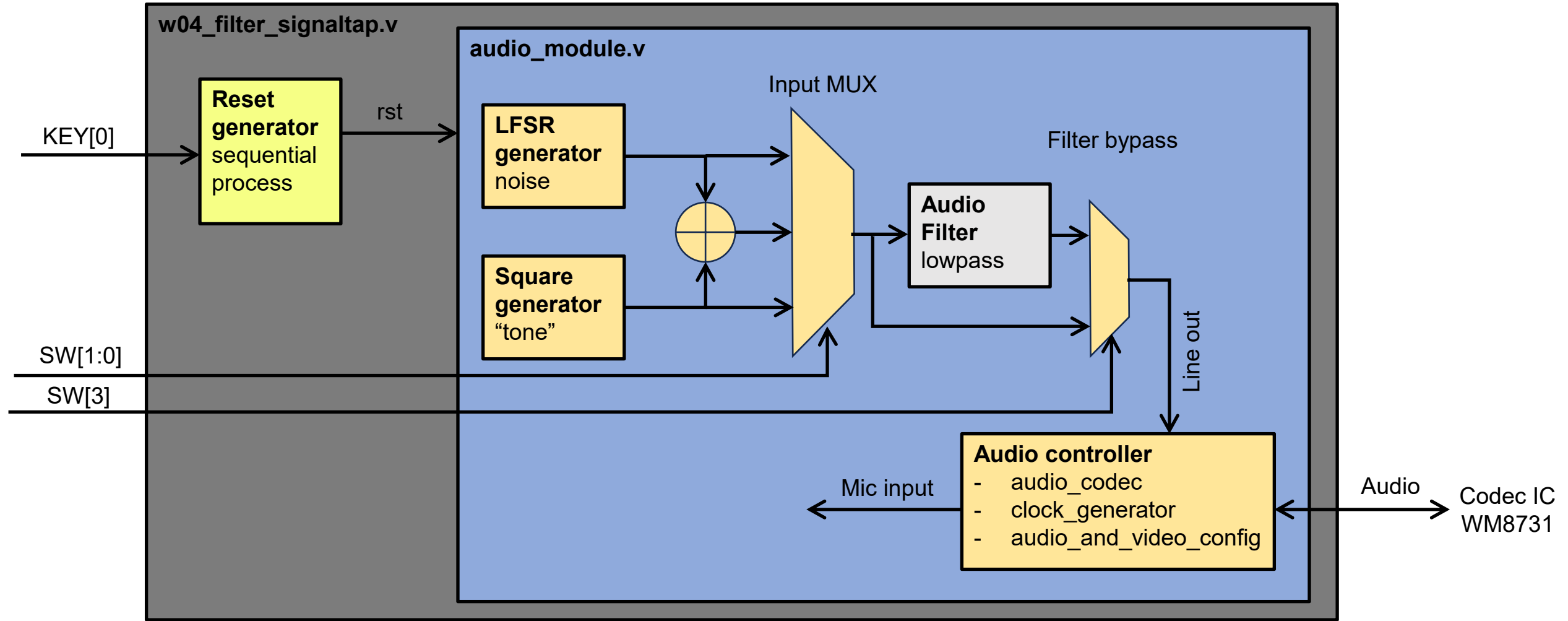


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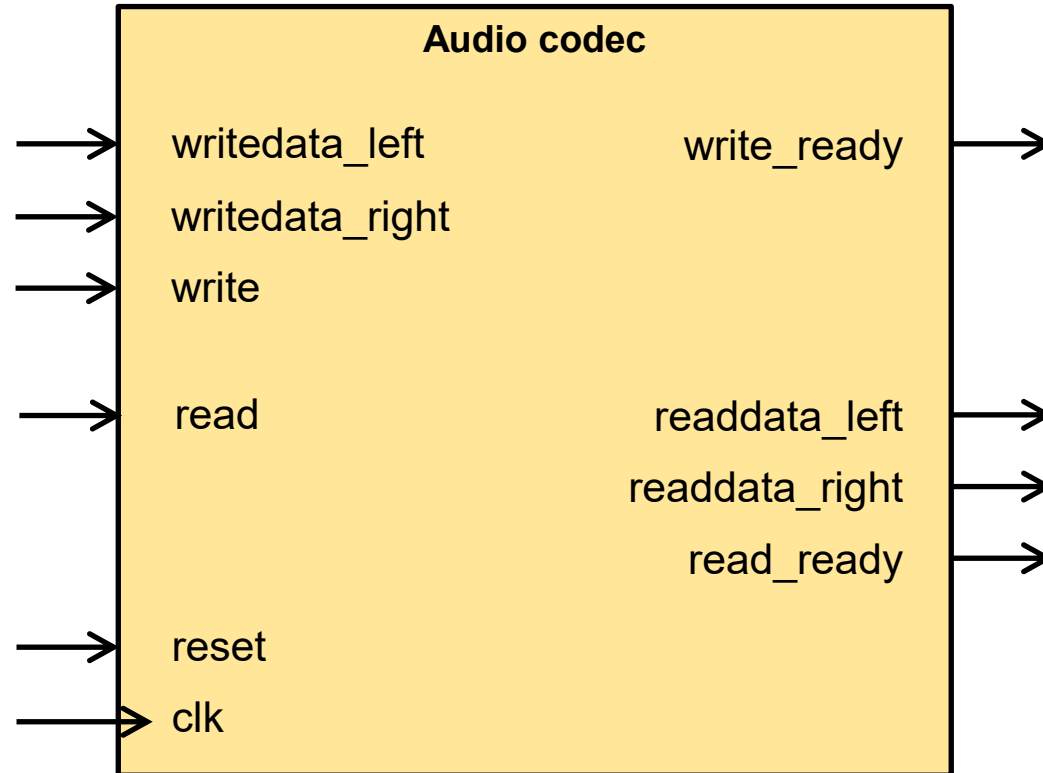
PA221: Filter and Signal Tap – Part 1

Template

Audio



Audio Codec



Assignment

Compile and load FPGA binary into EvalBoard

Signal Tap

- Examine all internal signal (previous slide) of Audio Codec
- Determine sampling frequency of **readdata_left** and **readdata_right** signals
- Set input mux to $SW[1:0] = 2'b01$ and capture at least one period of square wave signal in Signal Tap

Tips and Tricks

Task: Set input mux to $SW[1:0] = 2'b01$ and capture at least one period of square wave signal in Signal Tap

- Storage qualifier can be used to store only selected samples
- Bus format -> Signed line chart can be scaled if non-significant bits are removed from the bus

Tips and Tricks

The screenshot shows the Signal Tap Logic Analyzer interface. The main window displays a table of signals with columns for Data Enable, Trigger Enable, Storage Enable, Storage Qualifier, and Trigger Conditions. A red box highlights the Storage Qualifier column, which is set to 'Basic AND'. The Trigger Conditions column is also set to 'Basic AND'. The Signal Configuration panel on the right shows the Storage qualifier Type set to 'Conditional'.

	Data Enable	Trigger Enable	Storage Enable	Storage Qualifier	Trigger Conditions
	134	134	134	Basic AND	Basic AND
te_data[19]	✓	✓	✓	Basic AND	Basic AND
te_data[18]	✓	✓	✓	Basic AND	Basic AND
te_data[17]	✓	✓	✓	Basic AND	Basic AND
te_data[16]	✓	✓	✓	Basic AND	Basic AND
data[15..8]	✓	✓	✓	XXXXXXXXb	XXXXXXXXb
te_data[15]	✓	✓	✓	Basic AND	Basic AND
te_data[14]	✓	✓	✓	Basic AND	Basic AND
te_data[13]	✓	✓	✓	Basic AND	Basic AND
te_data[12]	✓	✓	✓	Basic AND	Basic AND

Tips and Tricks

The screenshot displays the Signal Tap Logic Analyzer interface. At the top, the title bar shows the file path and project name. The menu bar includes File, Edit, View, Project, Processing, Tools, Window, and Help. A search bar for Intel FPGA is visible on the right. Below the menu bar is a toolbar with various icons for file operations and analysis. The Instance Manager pane shows a table of instances:

Instance	Status	Enabled	LEs: 3557	Memory: 138240	Small: 0/0	Medium
auto_sigtap_0	Not running	<input checked="" type="checkbox"/>	3557 cells	138240 bits	0 blocks	14 blocks

The JTAG Chain Configuration pane on the right shows the hardware as DE-SoC [3-3] and the device as @2: 5CSE(BA5|MA5)/5. The main data log window shows a log entry for 2024/03/13 02:03:09. The log table has columns for Node, Type, Alias, Name, and time markers. A red box highlights the signal trace for the node `...odule:audio_module_inst|write_data[15..8]`. The Hierarchy Display pane at the bottom left shows the tree structure of the design, with the selected node expanded. The bottom right corner shows the zoom level at 100% and the time at 00:01:35.