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PV200

Introduction to hardware description languages

Week 02: Combination logic - Schematic, basic gates

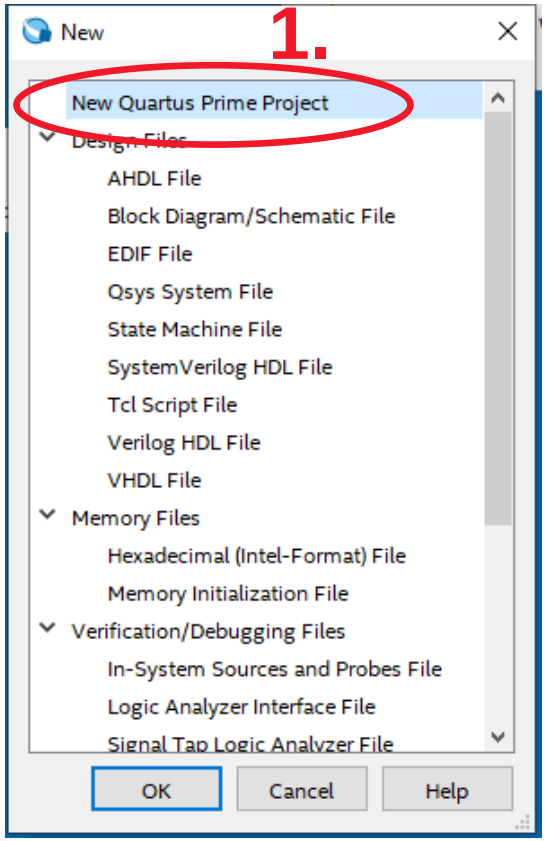
Ing. Jiří Čulen, 5.10.2021

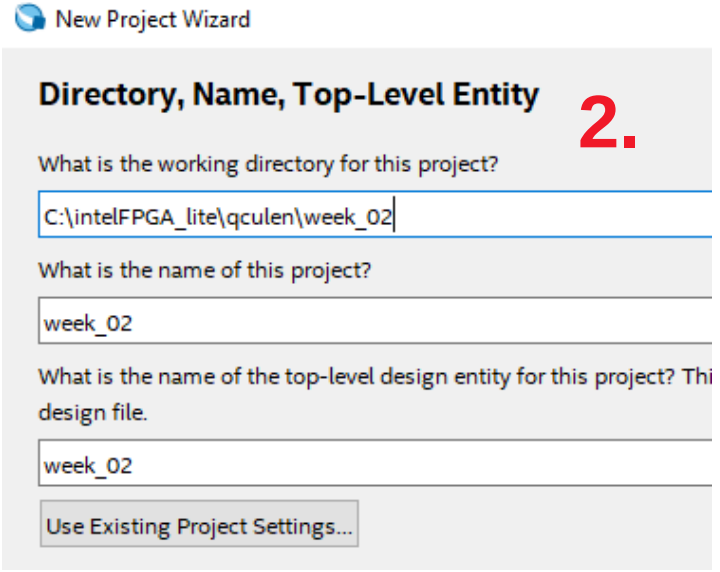
Agenda

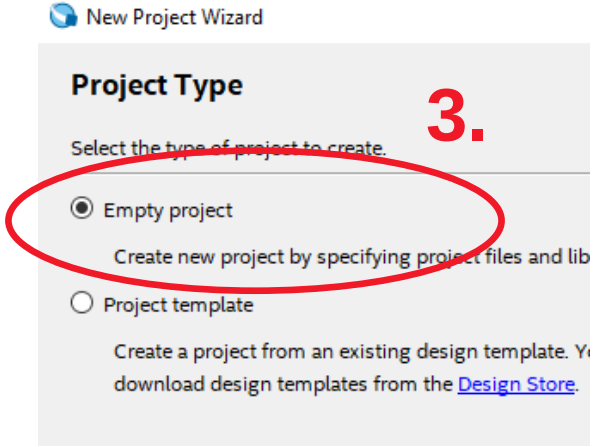
1. New empty project in the Quartus
2. Schematic editor
3. I/O settings
4. Programming the device
5. Half adder
6. Ful adder
7. Adding of two bits number

New empty project in the Quartus

- File -> New ->New Quartus Prime Project
- Select working directory and name of the project
- Define name of the project
- Project type – Empty project
- Skip add files







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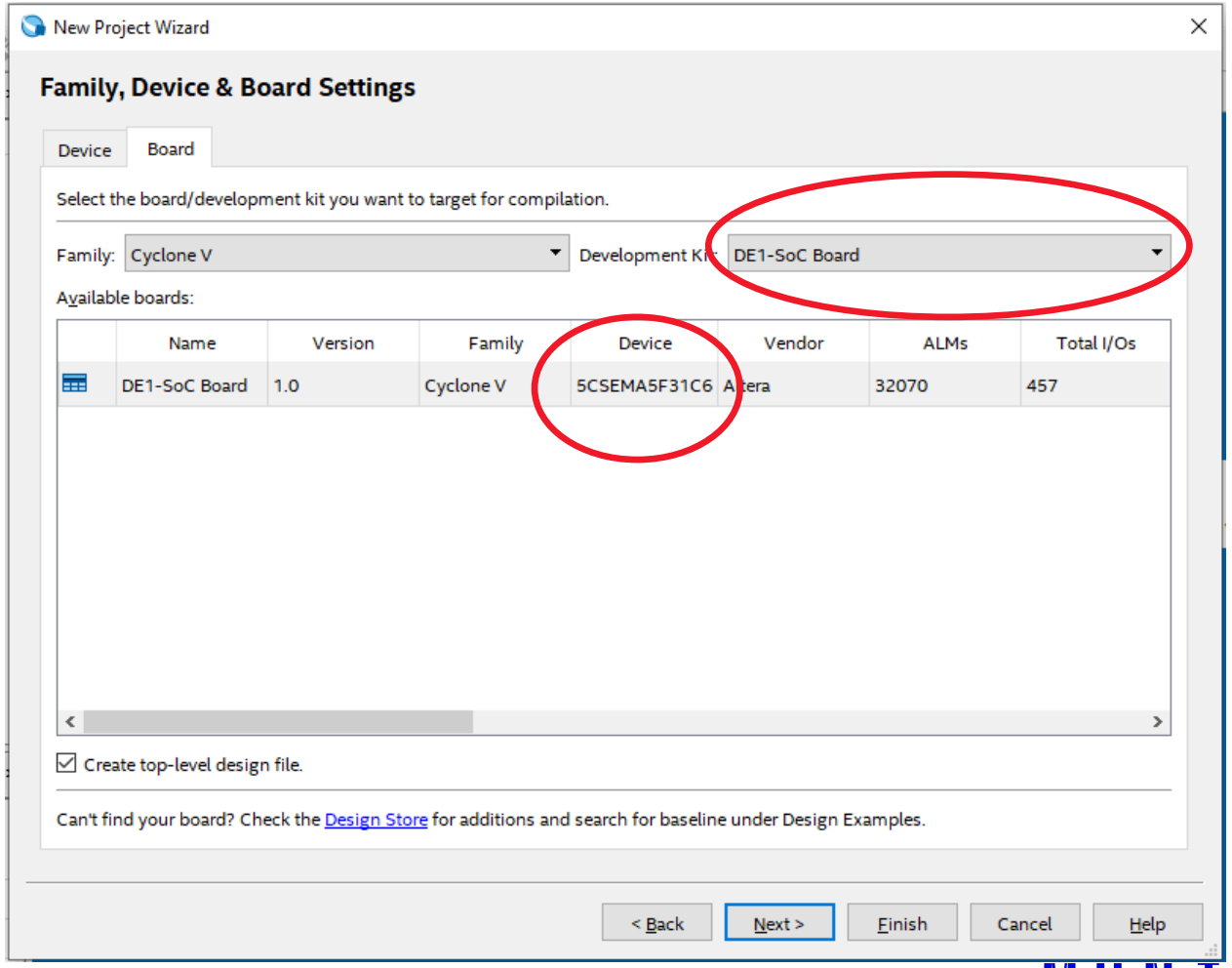
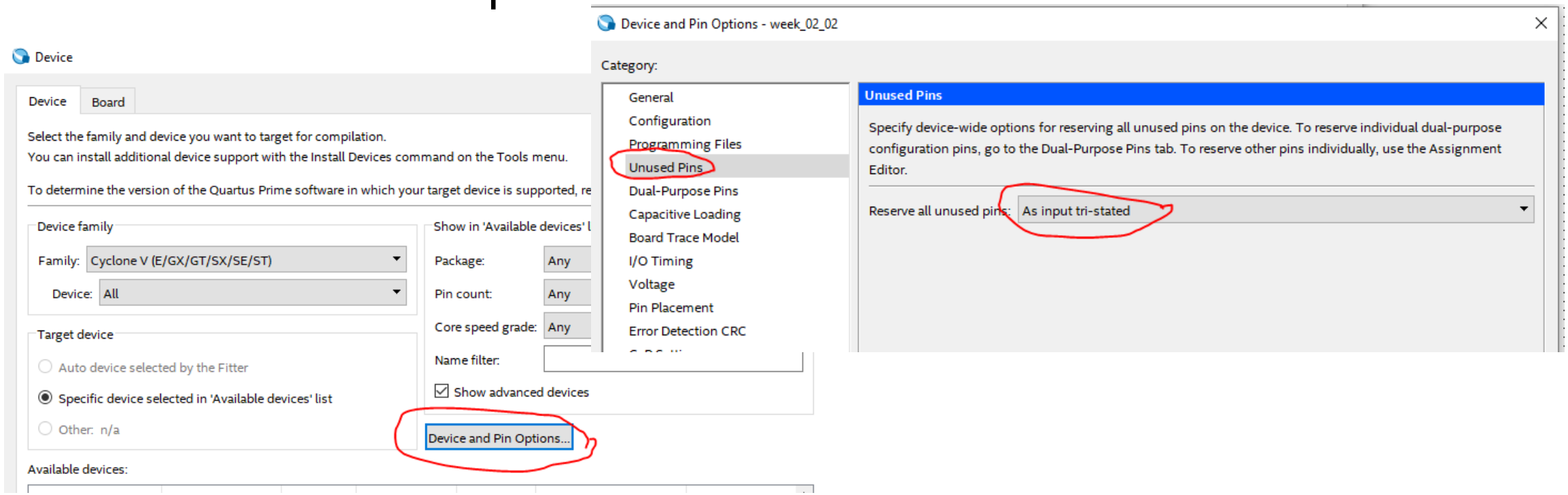
New empty project in the Quartus

- Select device from the Board DE1-SoC or manually 5CSEMA5F31C6
- Skip EDA Tool Settings
- Finish



New empty project in the Quartus

- Assignment -> Device -> Device and Pin Options
- Unused Pins -> As input tri-stated



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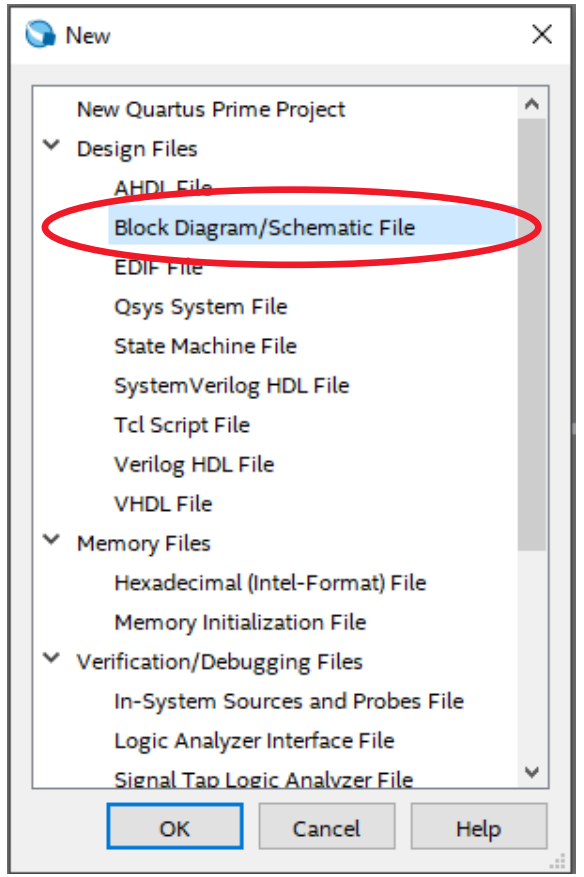
Schematic editor

- File -> New -> Block Diagram/Schematic File



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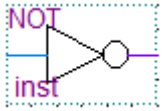
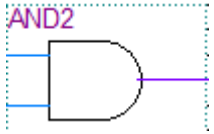
Schematic editor

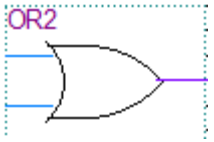
- We will need four basic gates



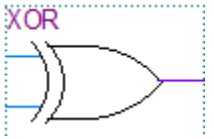
A	Q
0	1
1	0



A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

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Schematic editor

- We will use keys from the board, which are in negative logic. We need to invert it for positive logic.

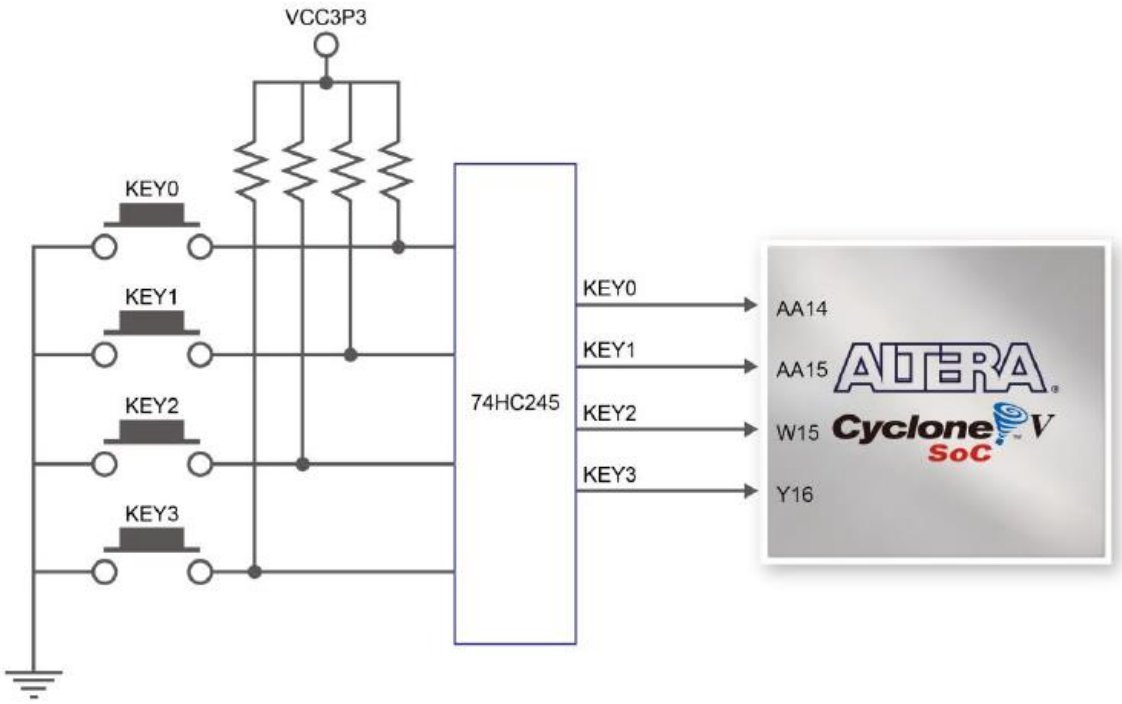

Figure 3-14 Connections between the push-buttons and the Cyclone V SoC FPGA

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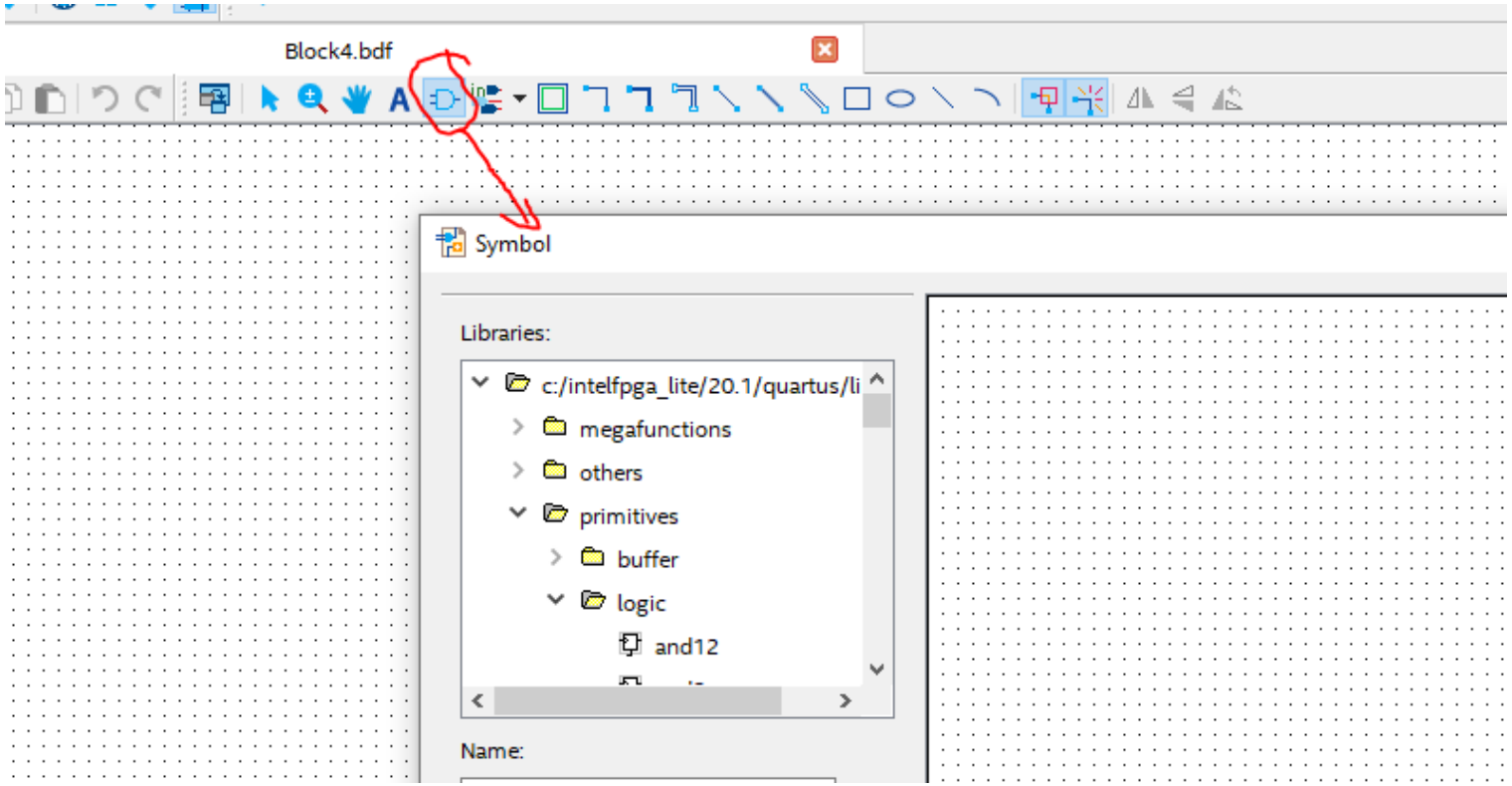
Schematic editor

- Place a symbol not



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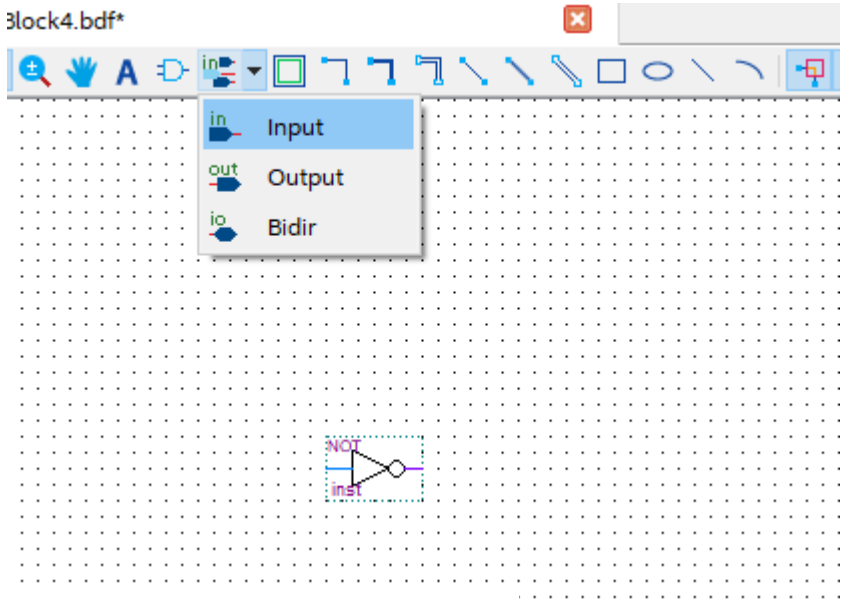
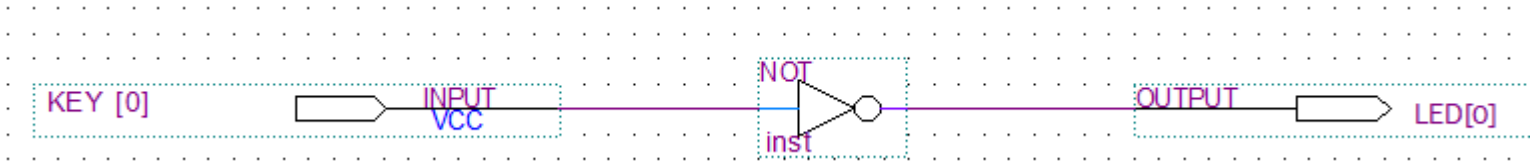
Schematic editor

- Place one input port and one output port and connect it to the NOT gate.
- The name of the input port will KEY[0], of the output LED[0].
- Save the schematic file.





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I/O settings

– Assignment of keys from the DE1-SoC manual

Table 3-7 Pin Assignment of Push-buttons

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
KEY[0]	PIN_AA14	Push-button[0]	3.3V
KEY[1]	PIN_AA15	Push-button[1]	3.3V
KEY[2]	PIN_W15	Push-button[2]	3.3V
KEY[3]	PIN_Y16	Push-button[3]	3.3V

I/O settings

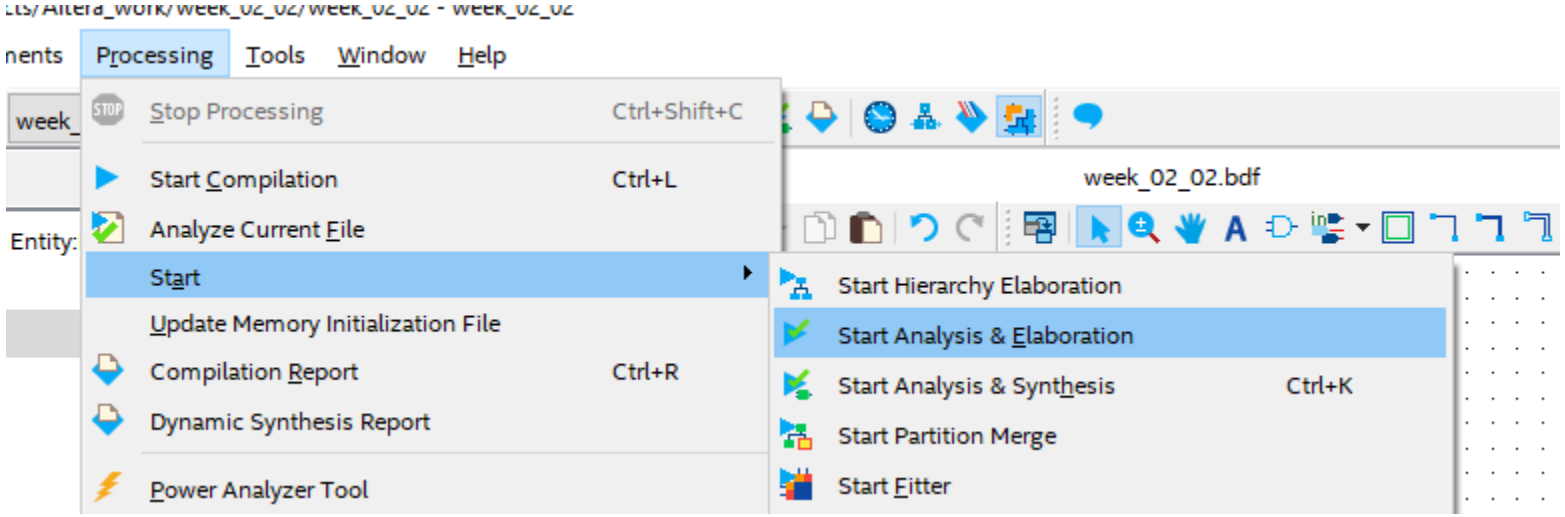
– Assignment of LEDS from the DE1-SoC manual

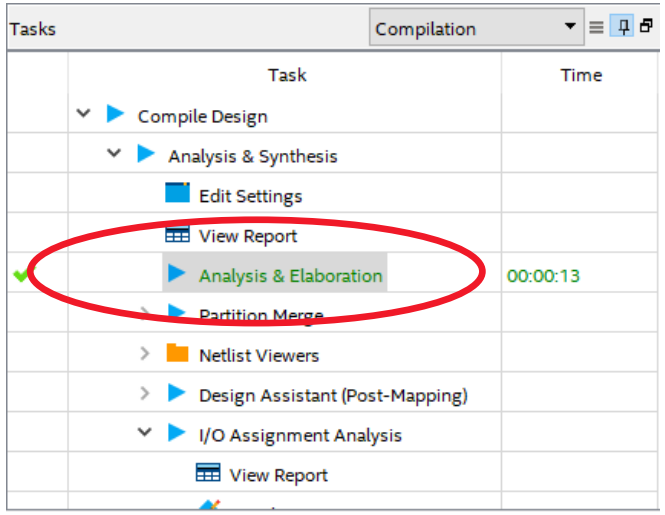
Table 3-8 Pin Assignment of LEDs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LEDR[0]	PIN_V16	LED [0]	3.3V
LEDR[1]	PIN_W16	LED [1]	3.3V
LEDR[2]	PIN_V17	LED [2]	3.3V
LEDR[3]	PIN_V18	LED [3]	3.3V
LEDR[4]	PIN_W17	LED [4]	3.3V
LEDR[5]	PIN_W19	LED [5]	3.3V
LEDR[6]	PIN_Y19	LED [6]	3.3V
LEDR[7]	PIN_W20	LED [7]	3.3V
LEDR[8]	PIN_W21	LED [8]	3.3V
LEDR[9]	PIN_Y21	LED [9]	3.3V

I/O settings

– Processing -> Start -> Start Analysis & Elaboration





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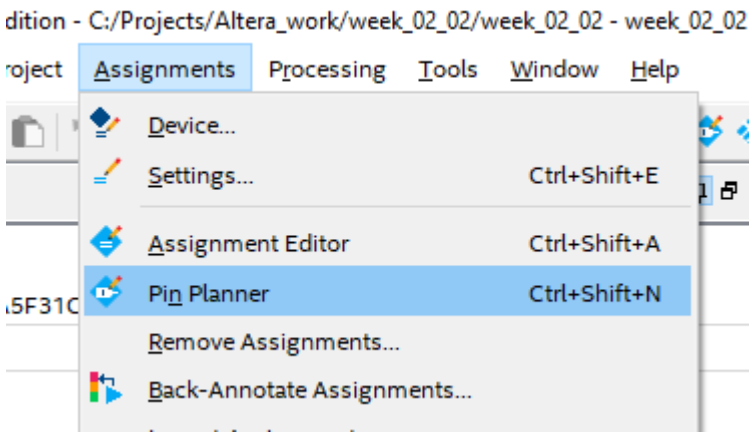
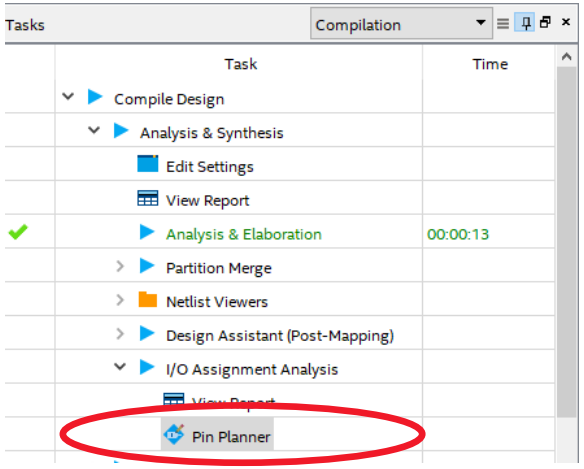
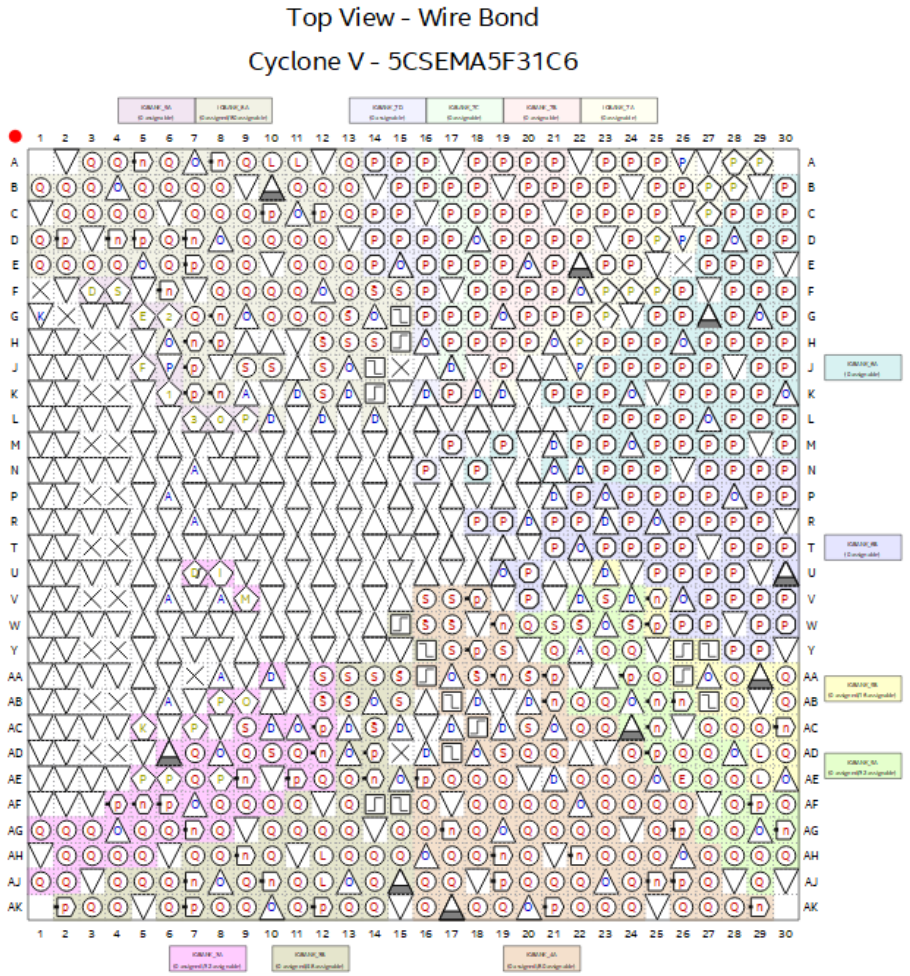
I/O settings

– Assignments -> Pin Planner







– Set the right parameters for our pins

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Diff
in KEY[0]	Input	PIN_AA14	3B	B3B_N0	3.3-V LVCMOS		2mA (default)		
out LED[0]	Output	PIN_V16	4A	B4A_N0	3.3-V LVCMOS		2mA (default)	0	
<<new node>>									

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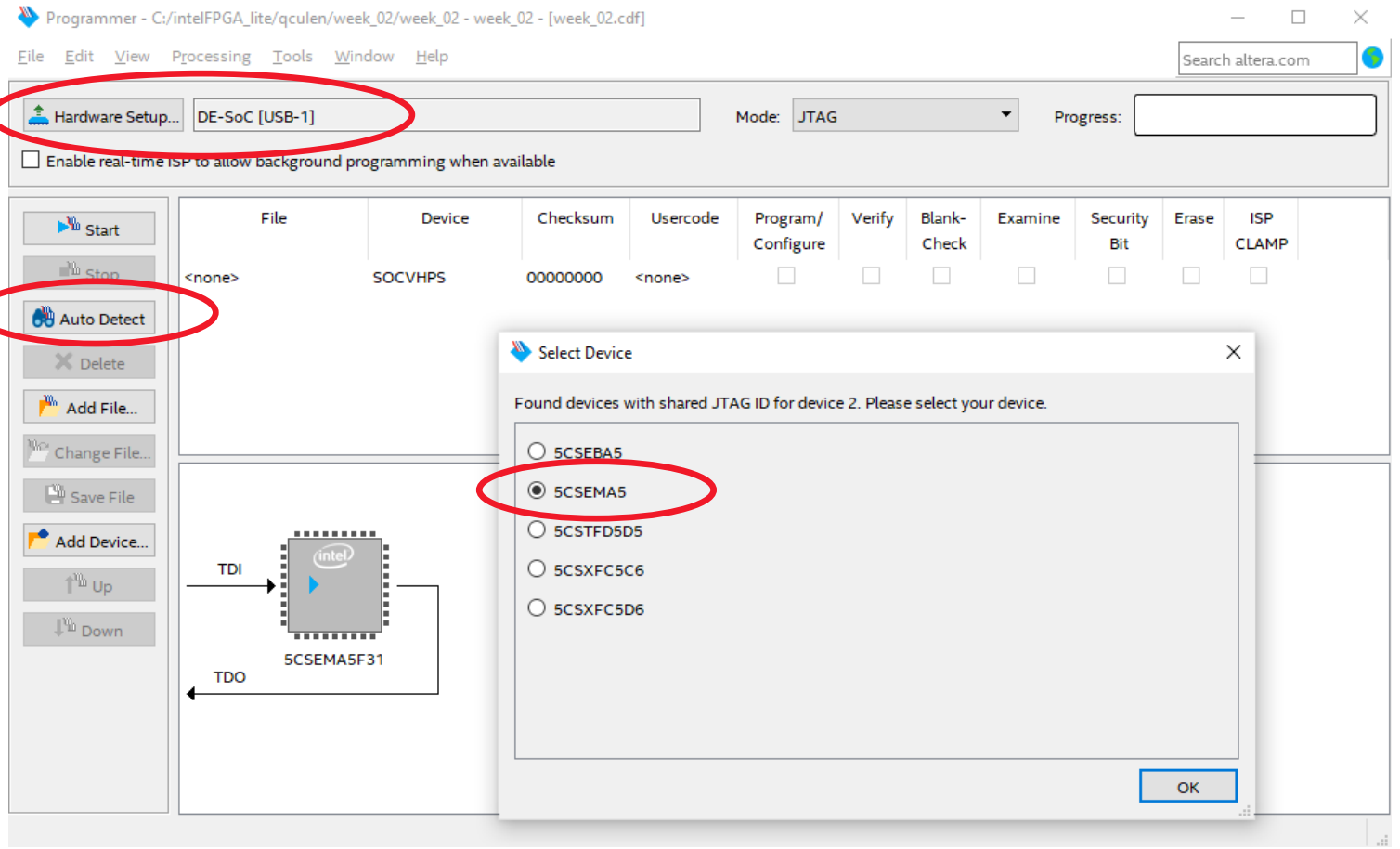
Programming the device

- Compile the project
- Open the programmer
- Check connection to the DE SoC board
- Select 5CSEMA5
- Detect your FPGA



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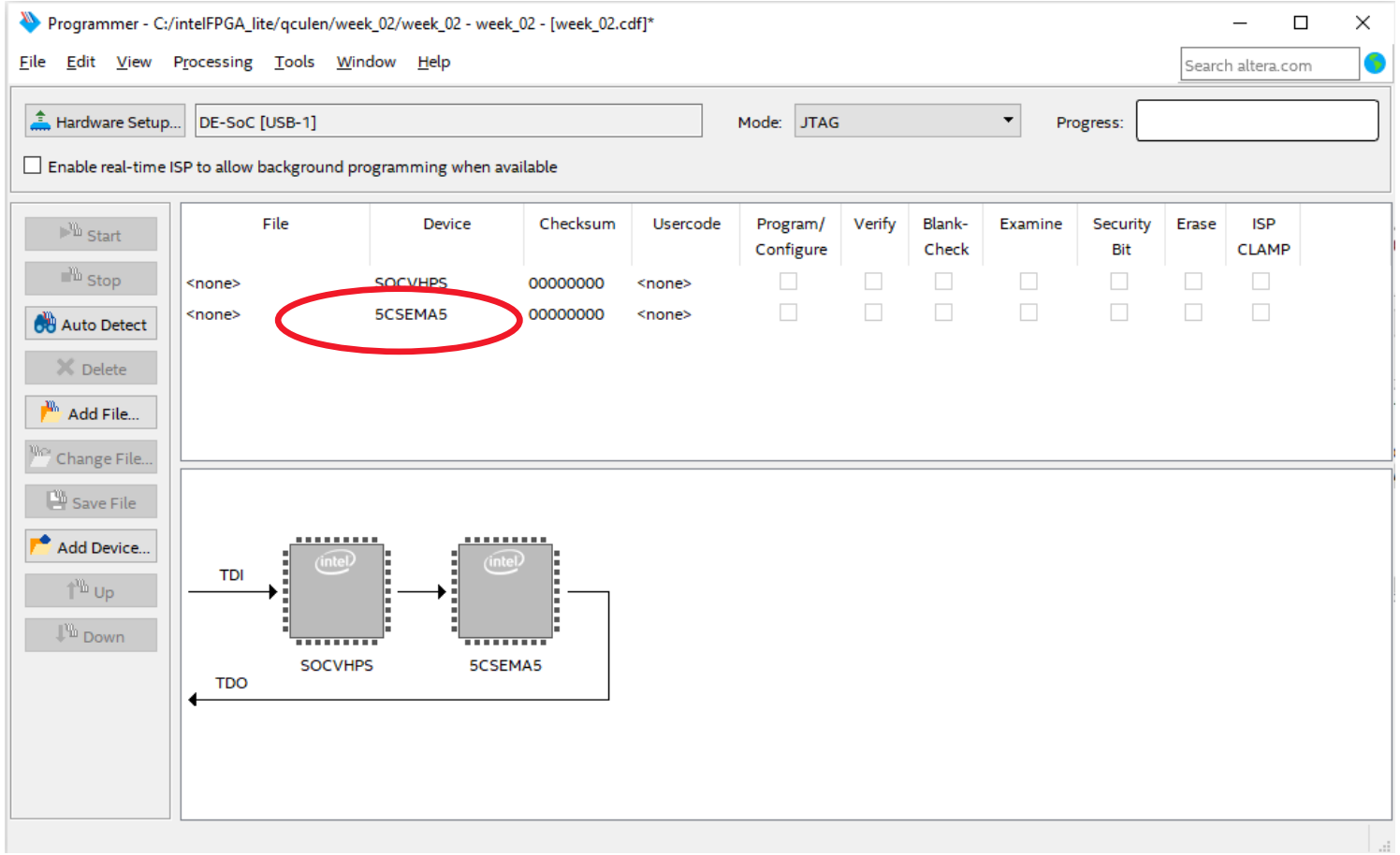
Programming the device

– FPGA 5CSEMA5 is detected



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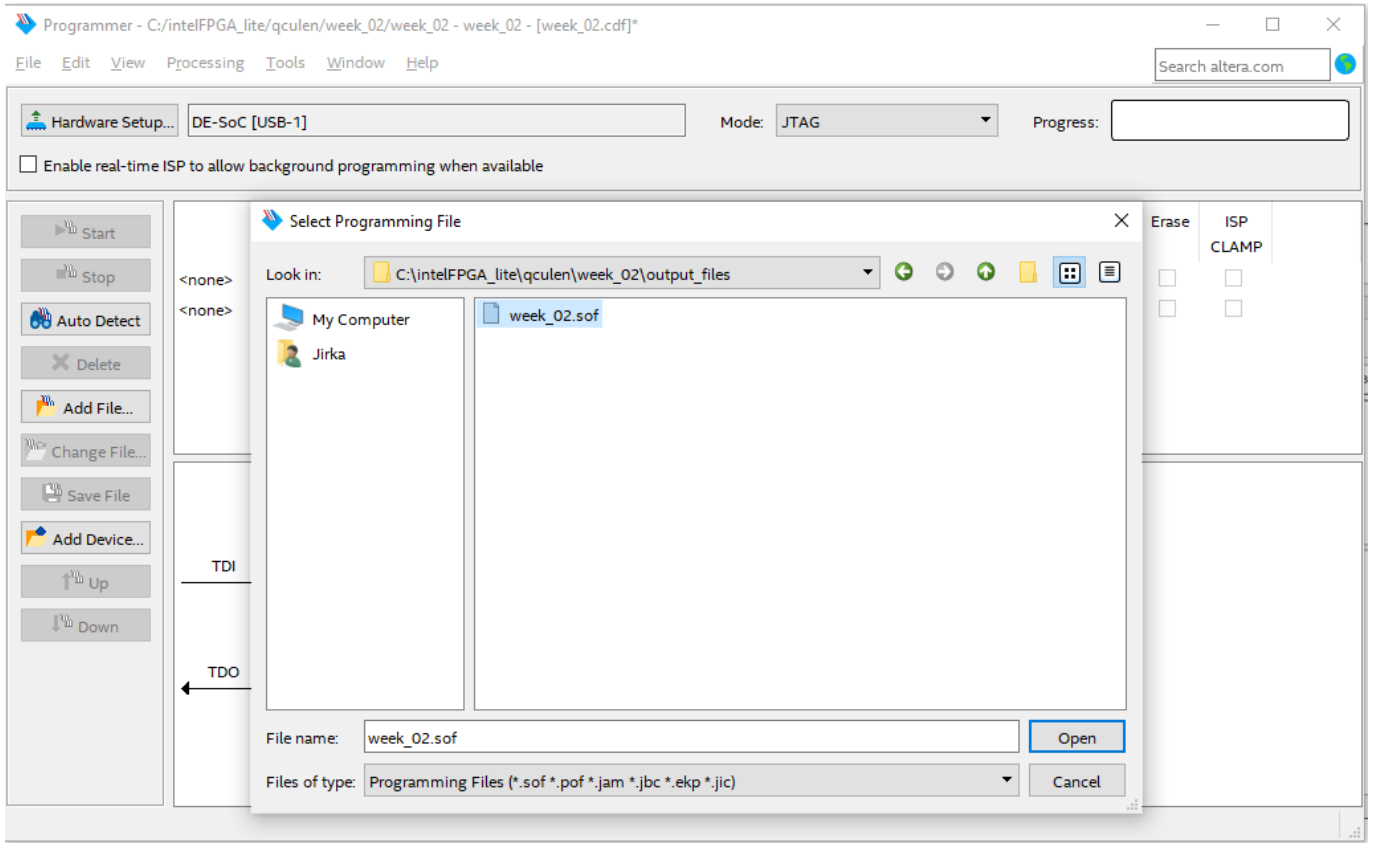
Programming the device

– Add file to the 5CSEMA5 device from the project



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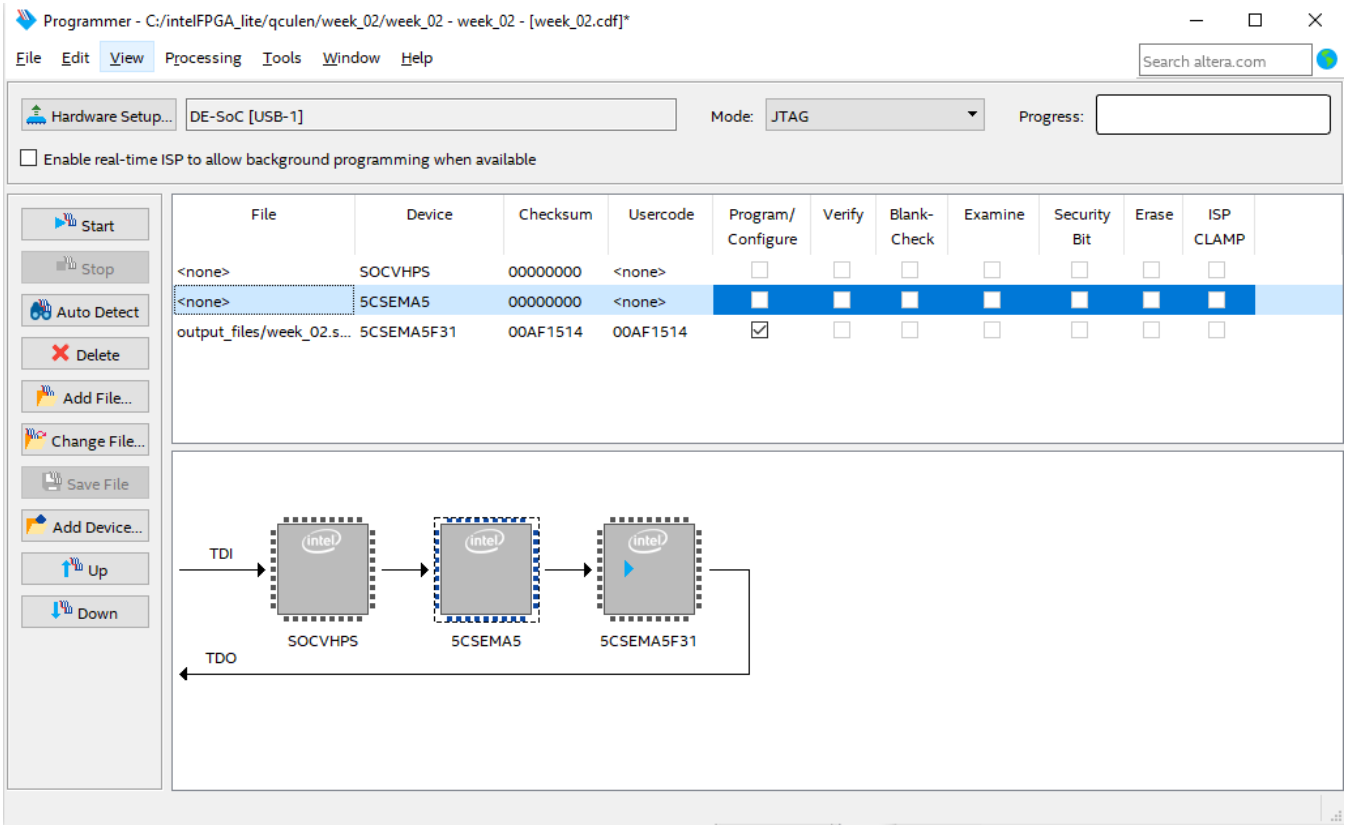
Programming the device

– Delete device 5CSEMA5



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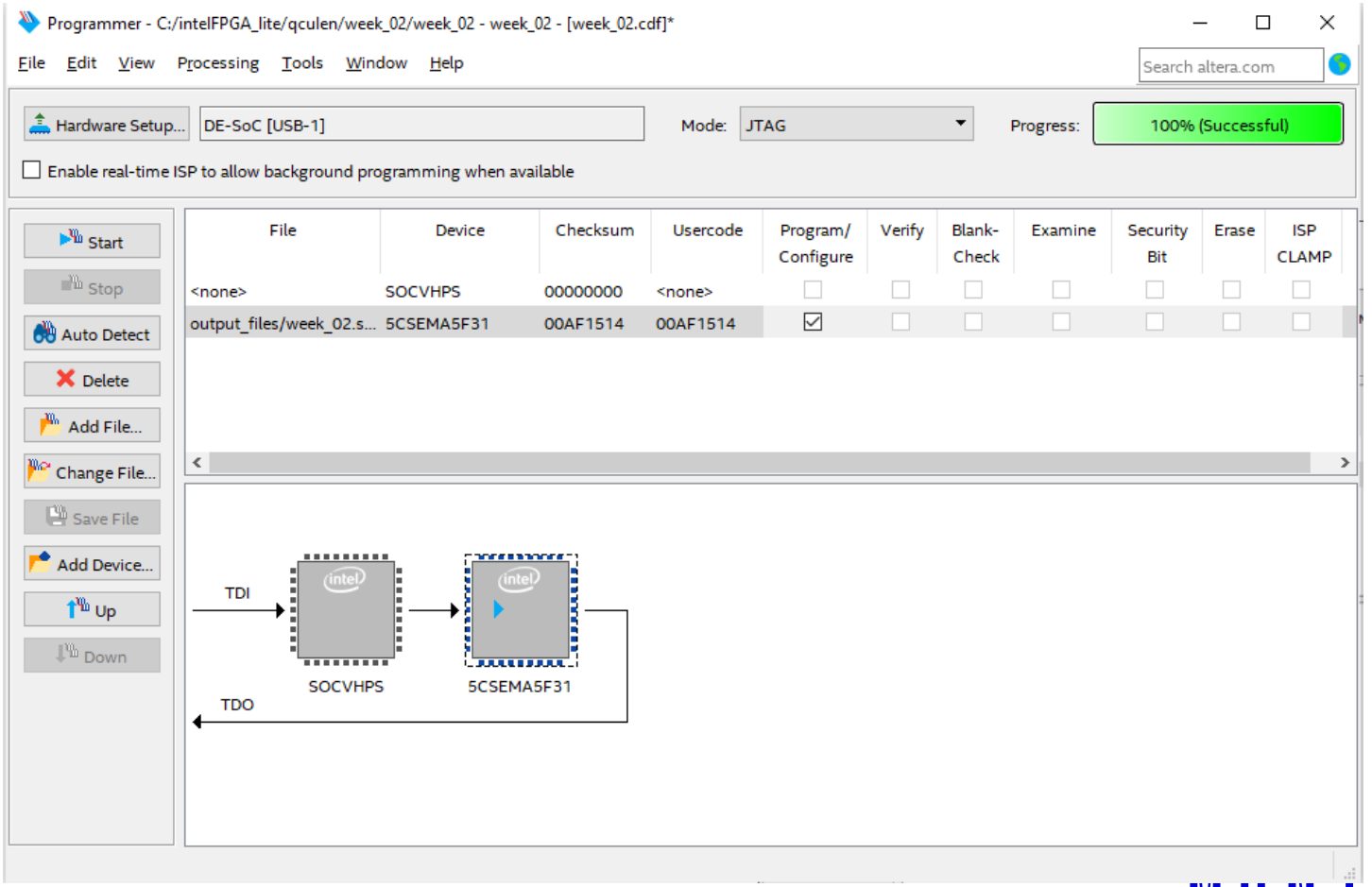
Programming the device

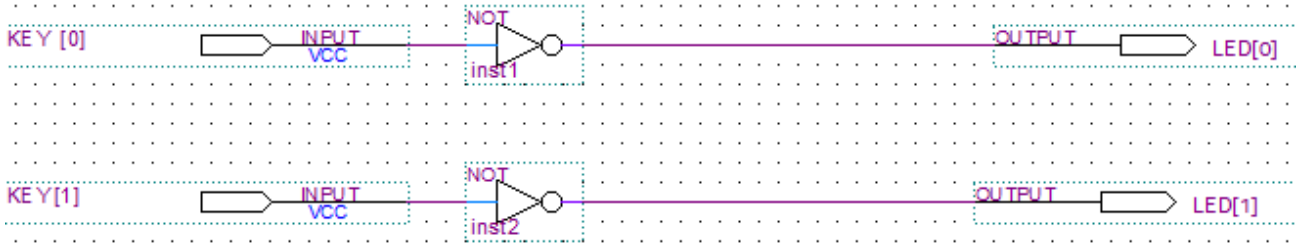
- Select 5CSEMA5F31
- Start the programming

- Test your application



Half adder

- Add the next pair of KEY and LED.
- For loading new ports to the I/O planner, You need repeat start of the Analysis & Elaboration
- Compile it and test it.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
in KEY[1]	Input	PIN_AA15	3B	B3B_N0	PIN_AA15	3.3-V LVCMOS		2mA (default)	
in KEY[0]	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	3.3-V LVCMOS		2mA (default)	
out LED[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	3.3-V LVCMOS		2mA (default)	0
out LED[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	3.3-V LVCMOS		2mA (default)	0

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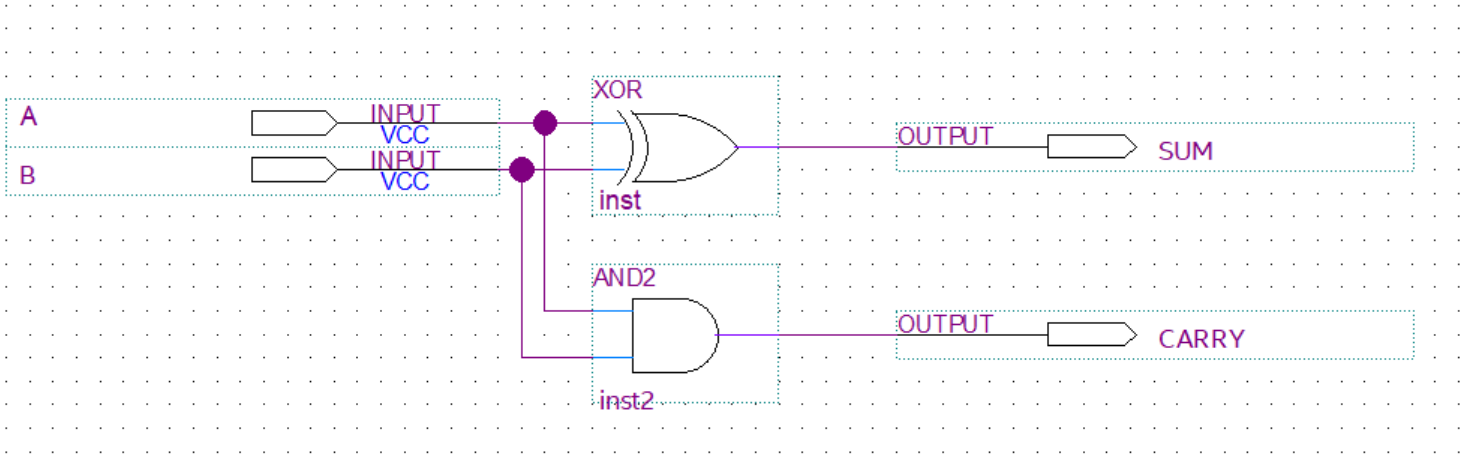
Half adder

- Create a new schematic file “half_adder”
- Use File -> Create/Update -> Create Symbol Files for Current File

A	B	SUM	CARRY
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1



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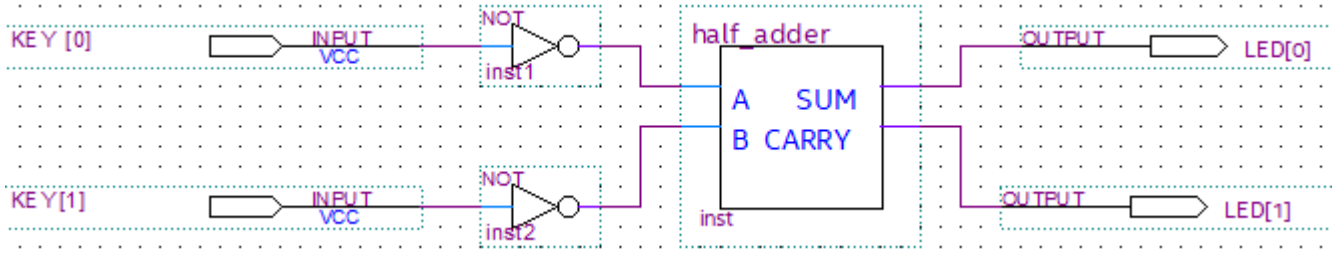
Half adder

- Put the half adder to the top schematic
- Compile it, program it, and test it…



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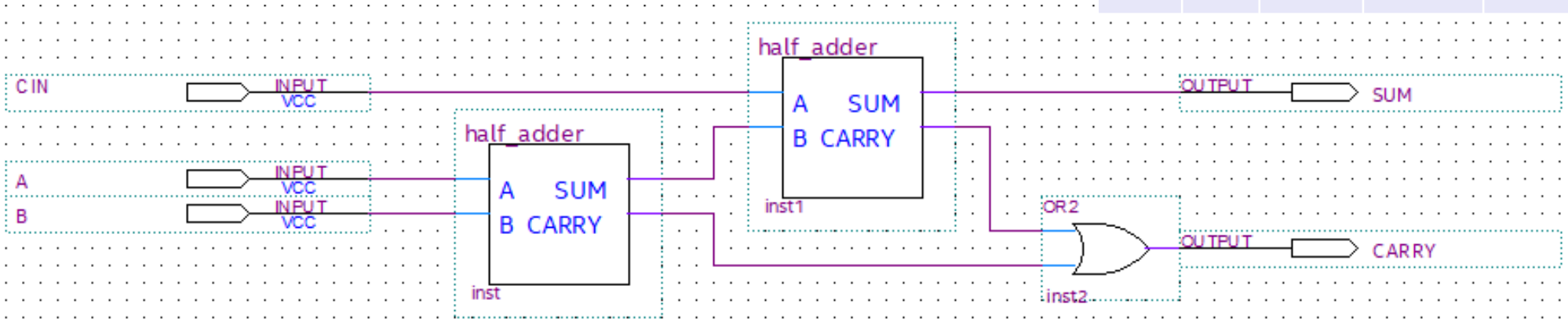
Full adder

- We can build full adder by using of half adders or by many others way…
- Create the new schematic file “full_adder”, and create symbol files

A	B	CIN	SUM	CARRY
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1



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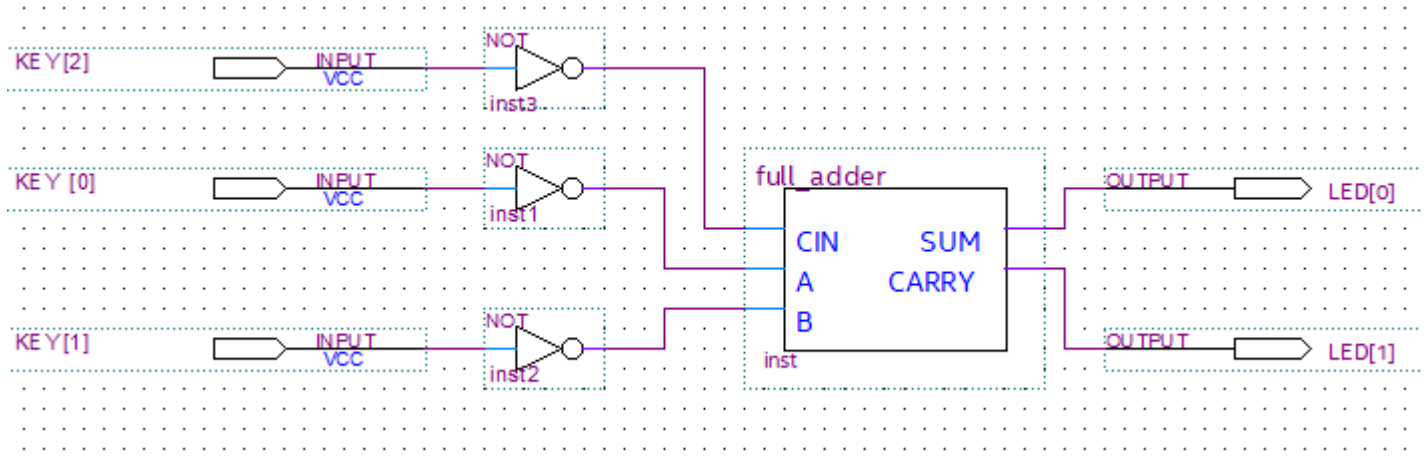
Full adder

- Put the half adder to the top schematic
- Compile it, program it, and test it…



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
in KEY[2]	Input	PIN_W15	3B	B3B_N0	PIN_W15	3.3-V LVCMOS		2mA (default)	
in KEY[1]	Input	PIN_AA15	3B	B3B_N0	PIN_AA15	3.3-V LVCMOS		2mA (default)	
in KEY[0]	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	3.3-V LVCMOS		2mA (default)	
out LED[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	3.3-V LVCMOS		2mA (default)	0
out LED[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	3.3-V LVCMOS		2mA (default)	0

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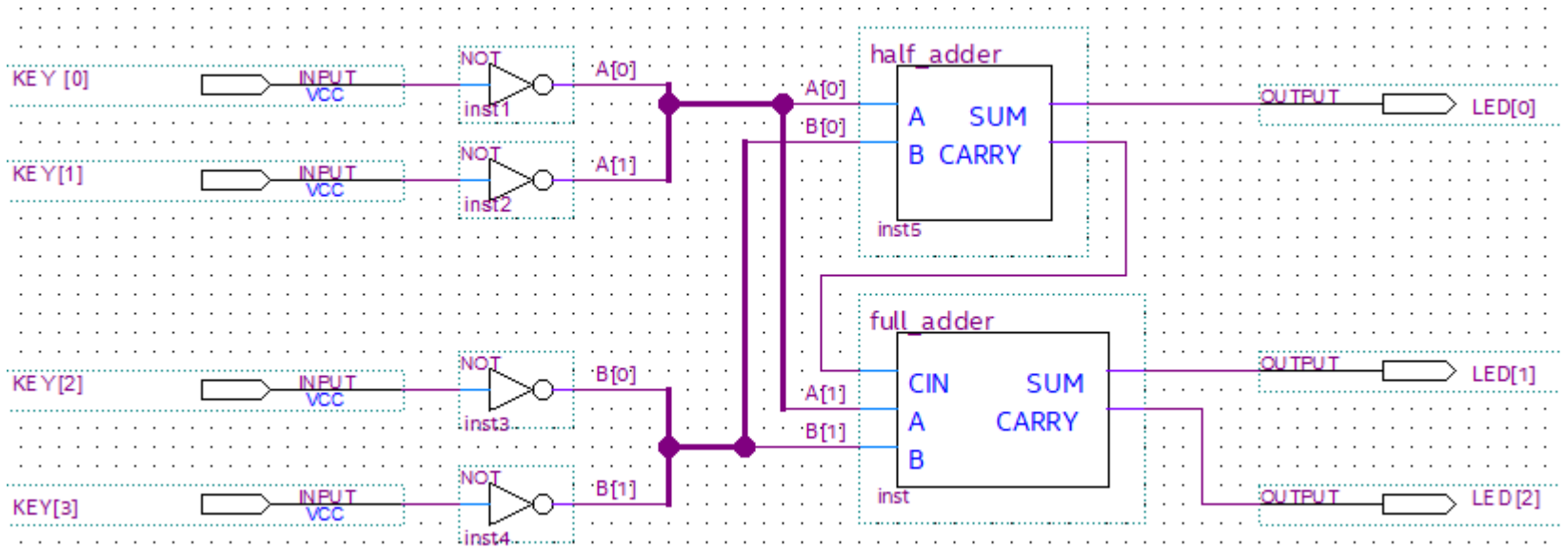
Adding of two bits number

- Modify the top schema and test it



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
KEY[3]	Input	PIN_Y16	3B	B3B_N0	PIN_Y16	3.3-V LVCMOS		2mA (default)	
KEY[2]	Input	PIN_W15	3B	B3B_N0	PIN_W15	3.3-V LVCMOS		2mA (default)	
KEY[1]	Input	PIN_AA15	3B	B3B_N0	PIN_AA15	3.3-V LVCMOS		2mA (default)	
KEY[0]	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	3.3-V LVCMOS		2mA (default)	
LED[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	3.3-V LVCMOS		2mA (default)	0
LED[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	3.3-V LVCMOS		2mA (default)	0
LED[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	3.3-V LVCMOS		2mA (default)	0

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Thank you for attention

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