PB173 Domain specific development: side-channel analysis

Trust, trusted element, usage scenarios, side-channel attacks
(shortened & based on PV204 lecture by P. Svenda)

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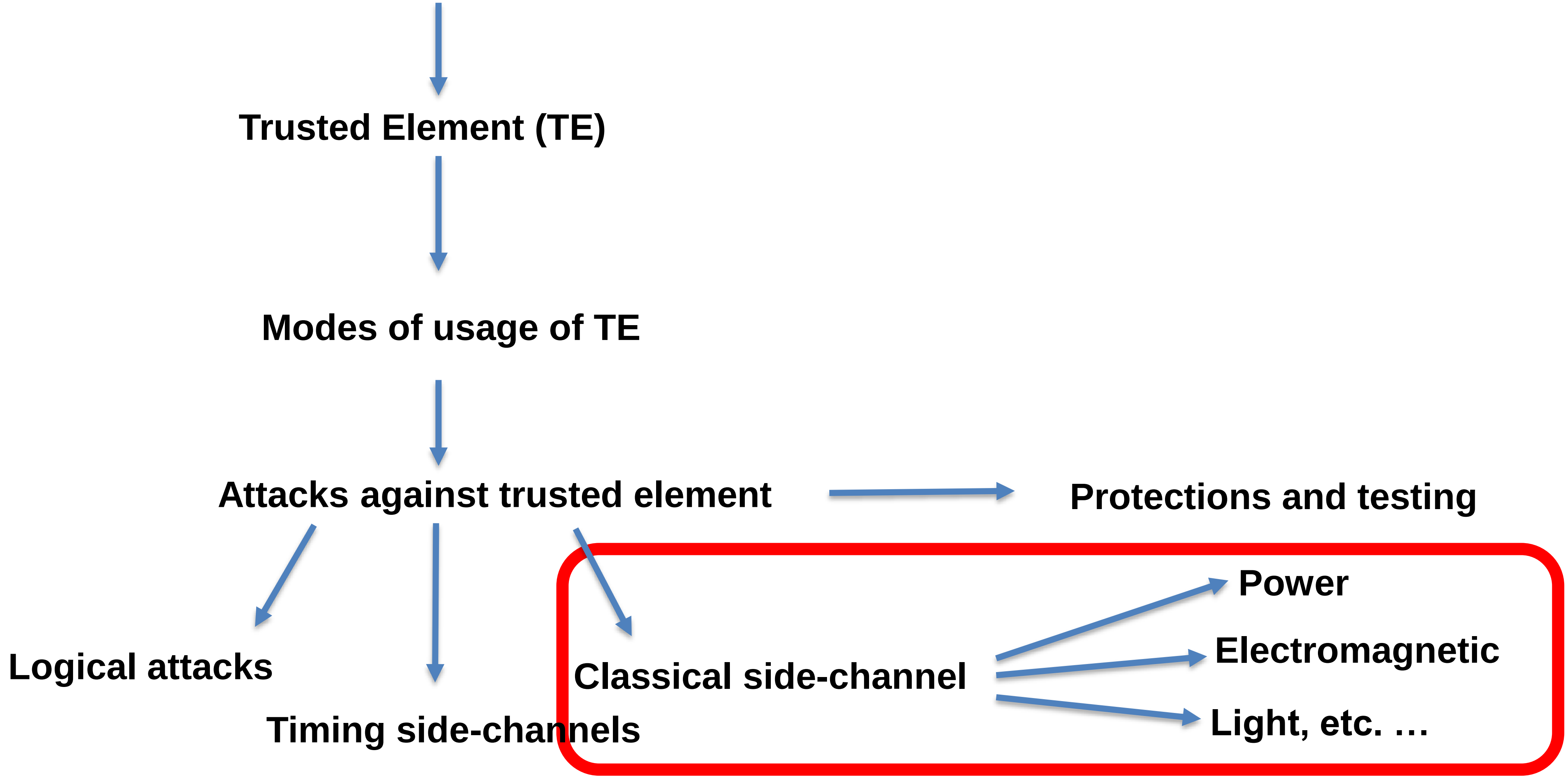
What is untrusted, trusted and trustworthy



Trusted system

- *"…system that is relied upon to a specified extent to enforce a specified security policy. As such, a trusted system is one whose failure may break a specified security policy."* (TCSEC, Orange Book)
- Trusted subjects are those excepted from mandatory security policies (Bell LaPadula model)
- User must trust (if wants to use the system)
  – E.g., you and your bank
- Trusted Computing Base

TRUSTED ELEMENT

What exactly can be trusted element (TE)?

- Recall: Anything user entity of TE is willing to trust ☺
  - Depends on definition of “trust” and definition of “element”
  - We will use narrower definition
- Trusted element is element (hardware, software or both) in the system intended to increase security *level* w.r.t. situation without the presence of such element
  1. By storage of sensitive information (keys, measured values)
  2. By enforcing integrity of execution of operation (firmware update)
  3. By performing computation with confidential data (DRM)
  4. By providing unforged reporting from untrusted environment (TPM)
  5. …

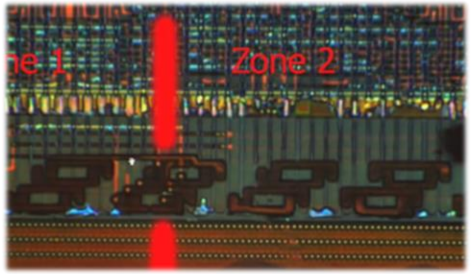
Typical examples

- Payment smart card
  - TE for issuing bank
- SIM card
  - TE for phone carriers
- Trusted Platform Module (TPM)
  - TE for user as storage of Bitlocker keys, TE for remote entity during attestation
- Trusted Execution Environment in mobile/set-top box
  - TE for issuer for confidentiality and integrity of code
- Hardware Security Module for TLS keys
  - TE for web admin
- Energy meter
  - TE for utility company
- Server under control of service provider
  - TE for user – private data, TE for provider – business operation
- Complex Scenarios: trusted element with (even more) trusted (crypto) hardware
  - TE for device manufacturer – secure derived keys, TE for chip manufacturer – secure root keys

For whom is TE trusted?

ATTACKS AGAINST TRUSTED ELEMENT

Trusted hardware (TE) is not panacea!



1. Can be physically attacked
   - Christopher Tarnovsky, BlackHat 2010
   - Infineon SLE 66 CL PE TPM chip, bus read by tiny probes
   - 9 months to carry the attack, $200k
   - https://www.youtube.com/watch?v=WXX00tRKOlw (great video with details)
2. Attacked via vulnerable API implementation
   - IBM 4758 HSM (Export long key under short DES one)
3. Provides trusted anchor != trustworthy system
   - Weakness can be introduced later
   - E.g., bug in newly updated firmware

Motivation: Bell's Model 131-B2 / Sigaba

- Encryption device intended for US army, 1943
  - Oscilloscope patterns detected during usage
  - 75 % of plaintexts intercepted from 80 feets
  - Protection devised (security perimeter), but forgot after the war
- CIA in 1951 – recovery over ¼ mile of power lines
- Other countries also discovered the issue
  - Russia, Japan…
- More research in use of (eavesdropping) and defense against (shielding) $\rightarrow$ TEMPEST

NON-INVASIVE LOGICAL ATTACKS

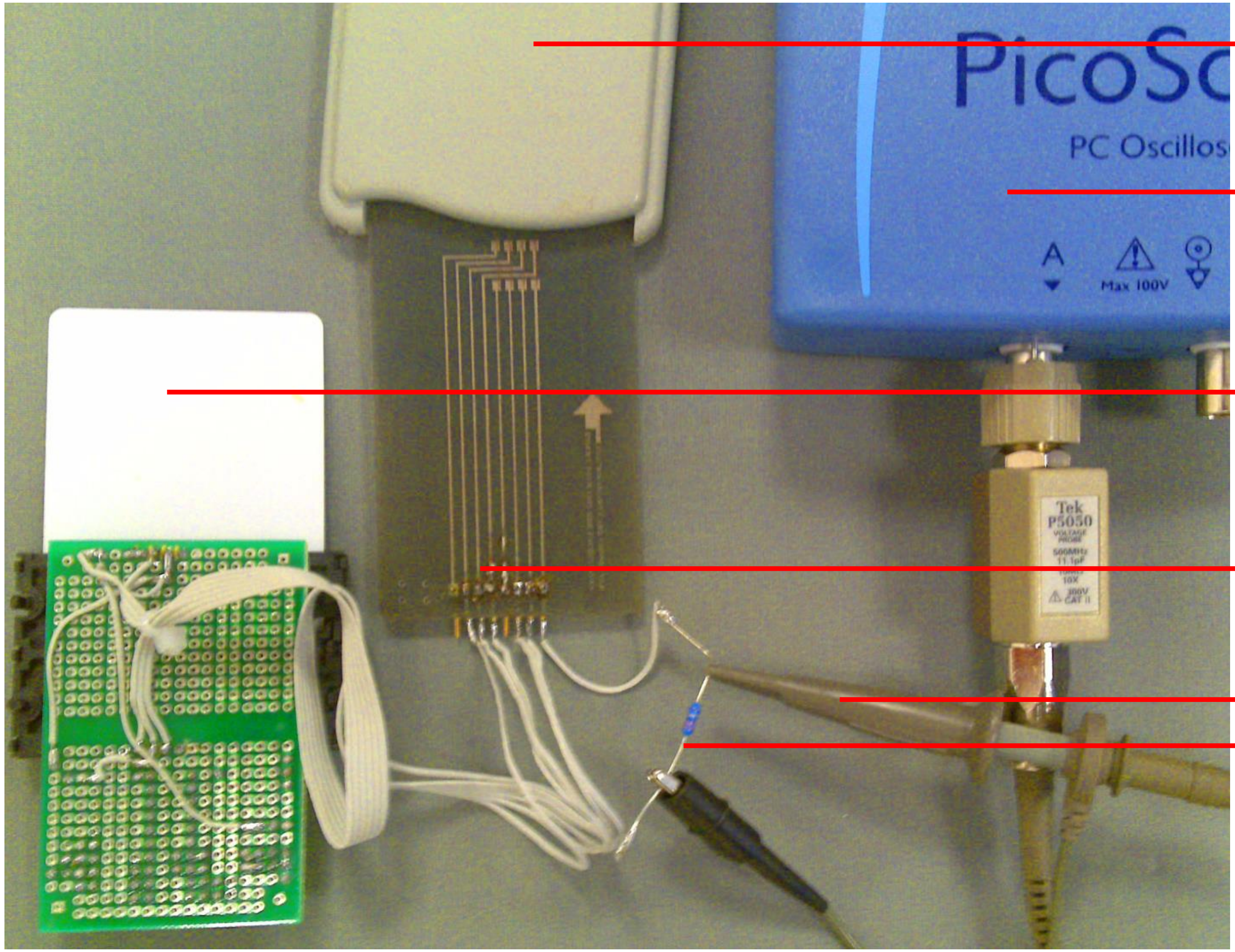
Non-complete list

- Algorithmic flaw in Infineon's RSALib (CVE-2017-15361)
  - RSA public / private key generation on many Infineon cards (huge impact)
  - https://keychest.net/roca, https://github.com/crocs-muni/roca/
- Not enforcing secure memory protections
  - A complete exploit on Set-top Boxes
  - Presented for two ST chips, but with impact on other ST chips too
  - https://www.youtube.com/watch?v=WF1wSzTTqdg&ab_channel=HackInTheBoxSecurityConference
- Shortening Key (against hardware key stores or key ladders):
  - Using half of an AES key as a DES key or using 3DES with half of the key (i.e., single DES key)
- TEE (e.g., ARM Trustzone) issues
  - Configuration, Memory Ranges, Boot ROM…
  - https://www.slideshare.net/CristofaroMune/euskalhack-2017-secure-initialization-of-tees-when-secure-boot-falls-short
  - …

Passive Side-Channel

SIDE-CHANNEL ANALYSIS

Basic setup for power analysis



Smart card reader

Oscilloscope

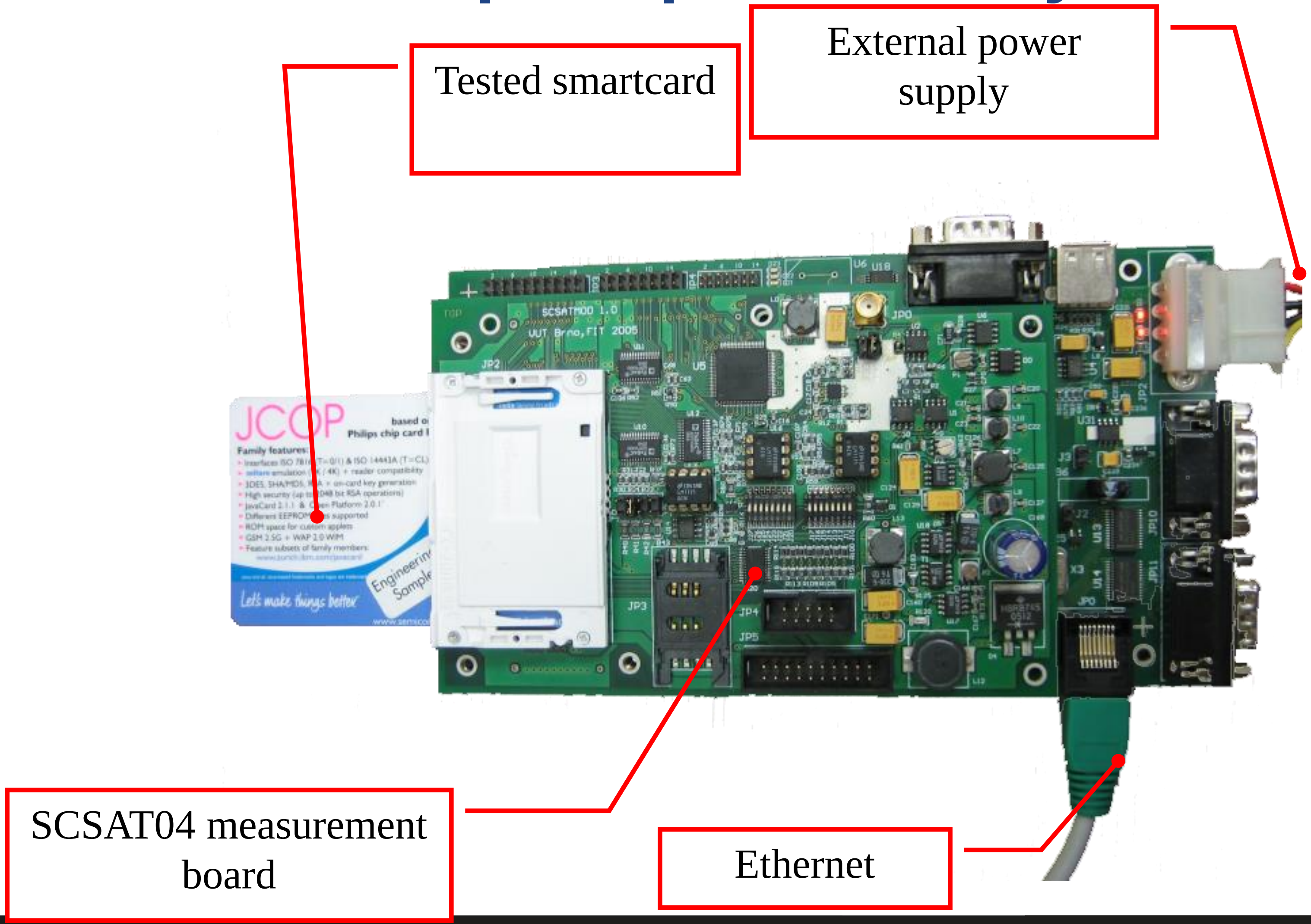
Smart card

Inverse card connector

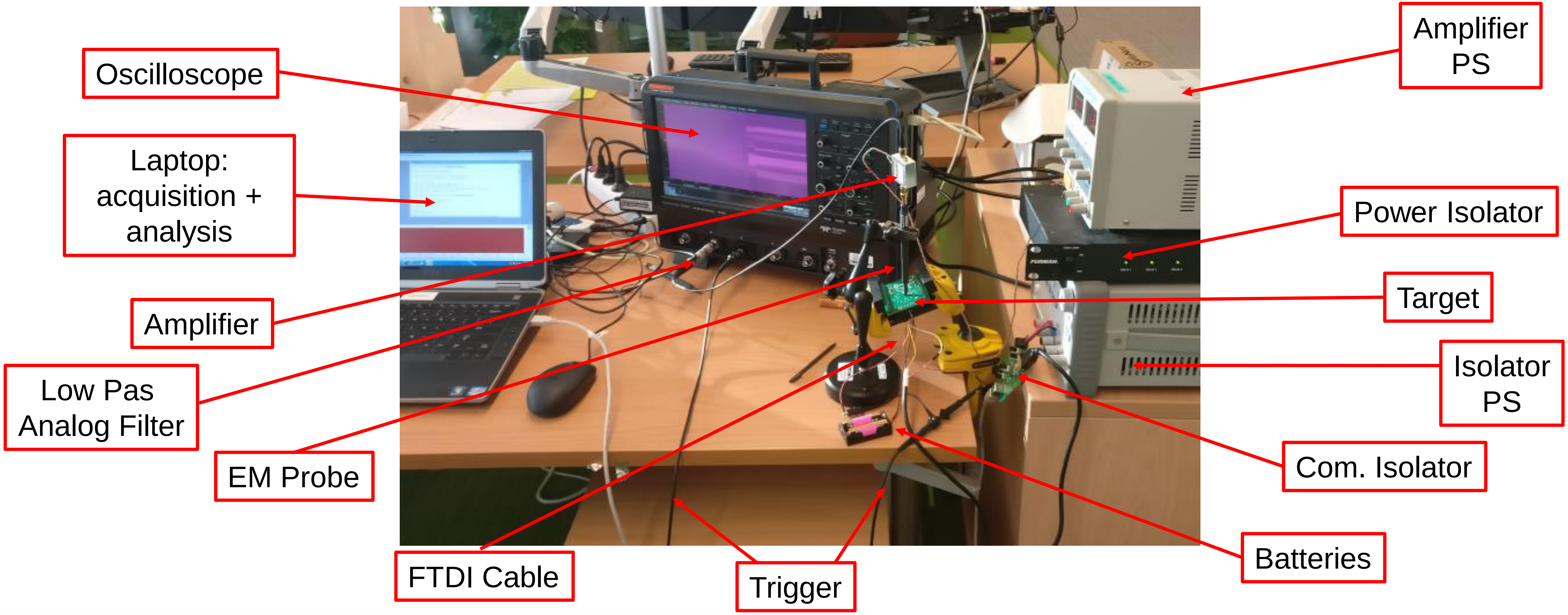
Probe

Resistor 20-80 ohm

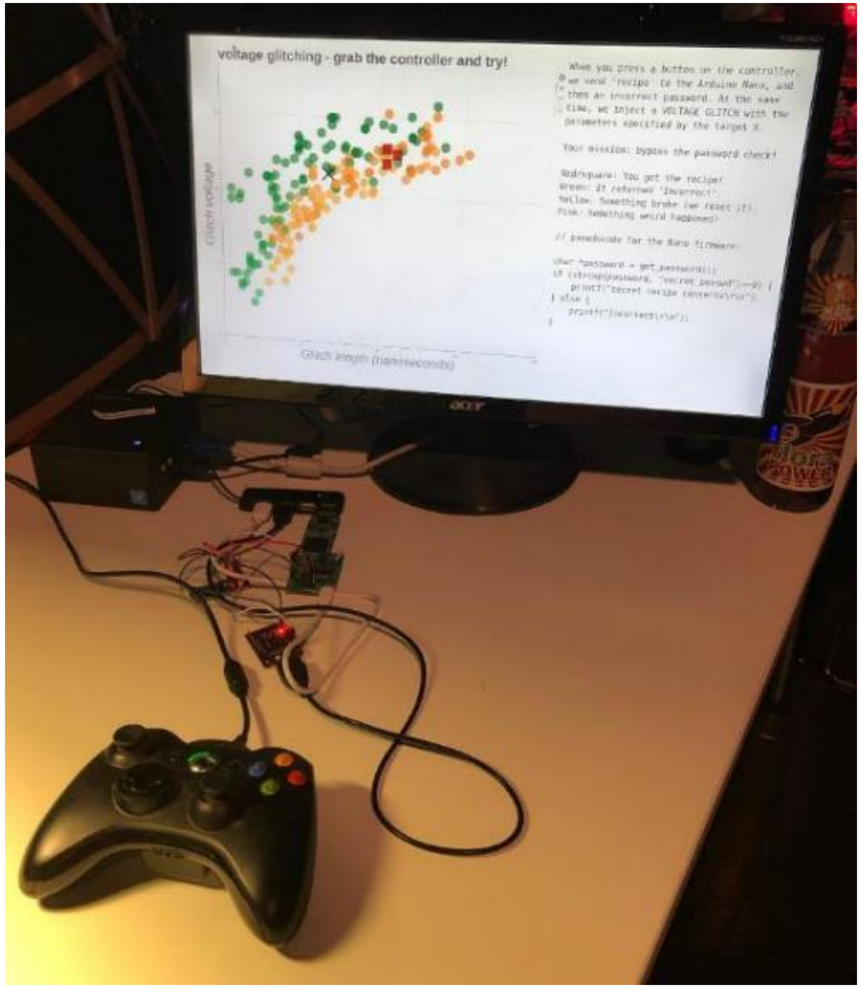
More advanced setup for power analysis



Even more advanced setup for EM analysis



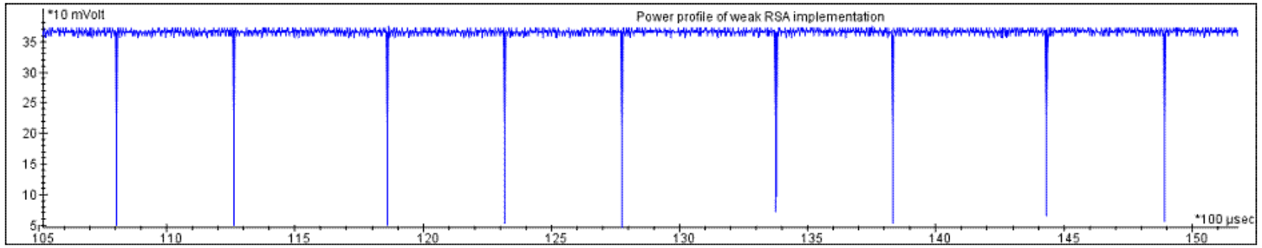
Simple (Cheap) Power Fault Injection setup



https://github.com/noopwafel/iceglitch

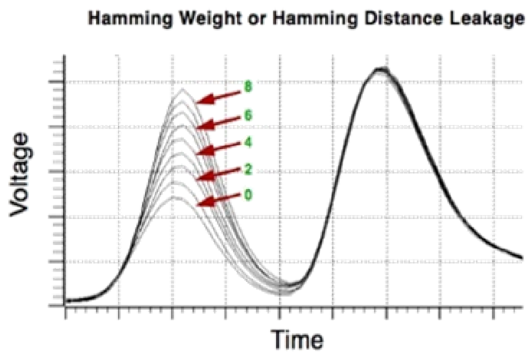
More on that in two weeks

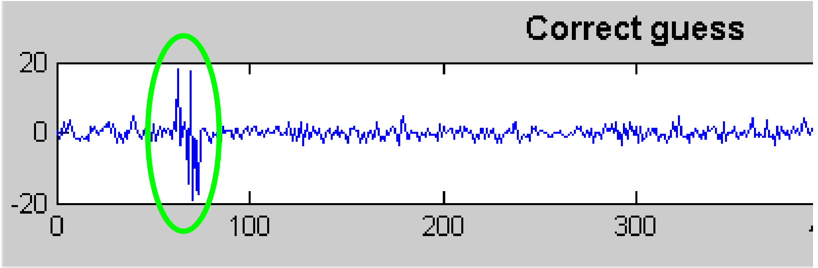
Simple vs. differential power analysis



https://www.riscure.com/uploads/2018/11/201708_Riscure_Whitepaper_Side_Channel_Patterns.pdf

1. Simple power analysis
   – Direct observation of single / few power traces
   – Visible operation => reverse engineering
   – Visible patterns => data dependency
2. Differential power analysis
   – Statistical processing of many power traces
   – More subtle data dependencies found

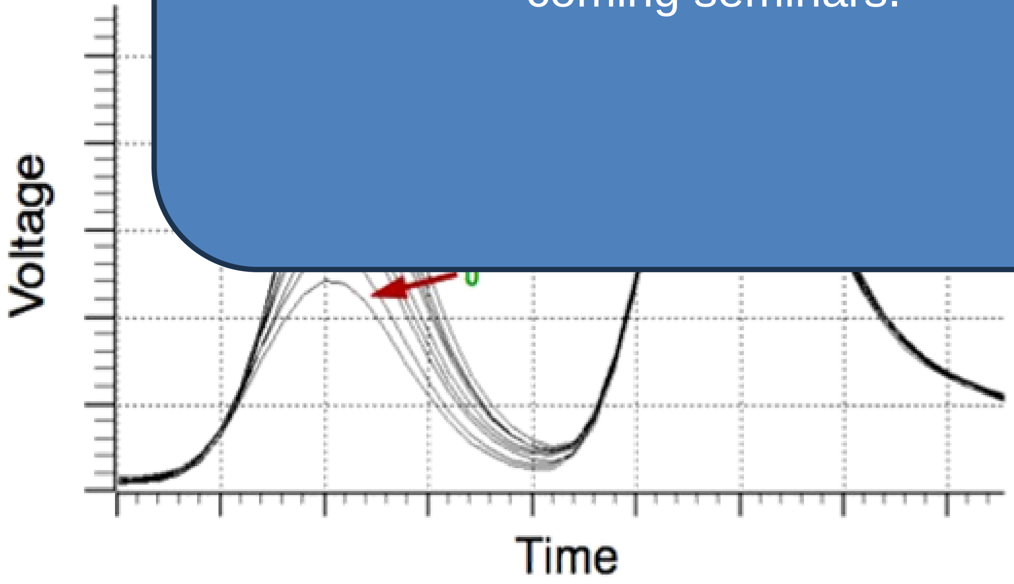




Simple power analysis – data leakage

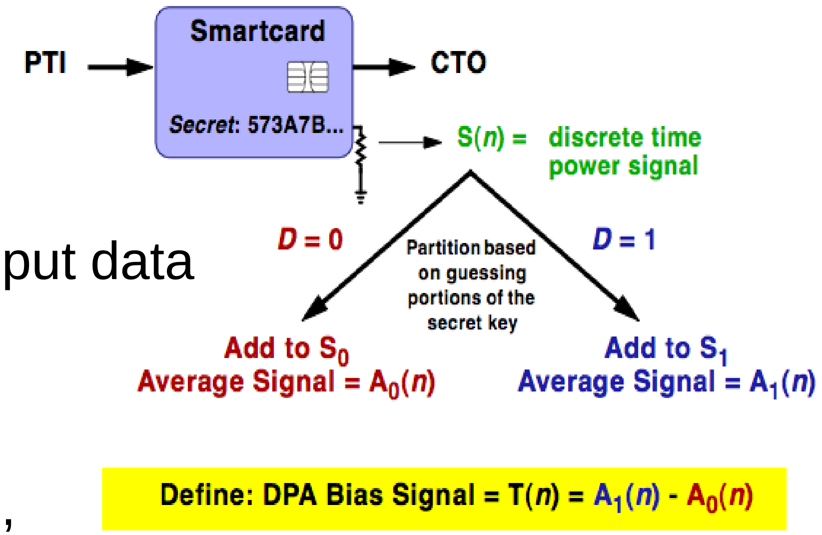
- Data revealed directly
  - e.g., Hamming weight
    - hamming weight of … is?

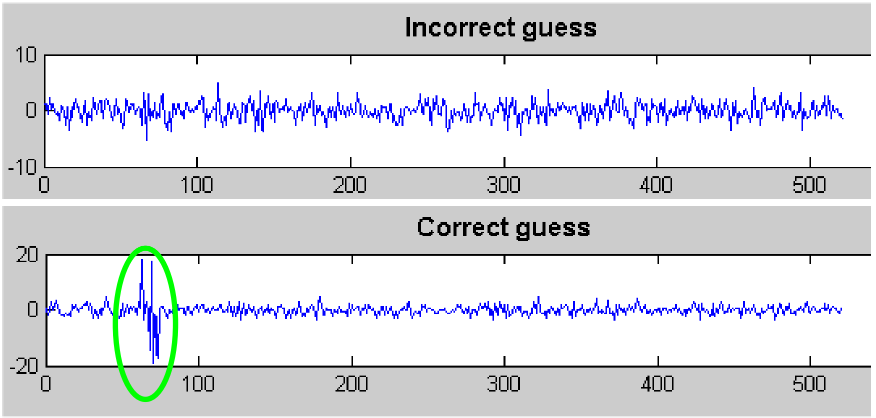
This is important and we will look into that in the coming seminars.



Differential power analysis (DPA)

- DPA attack recovers secret key (e.g., AES)
- Requires large number of power traces (10^2-10^6)
  - Every trace measured on AES key invocation with different input data
- Key recovered iteratively
  - One recovered byte at the time Sbox($KEY_i \oplus INPUT\_DATA_i$)
  - Guess possible key byte value (0-255), group measurements, compute average, determine match





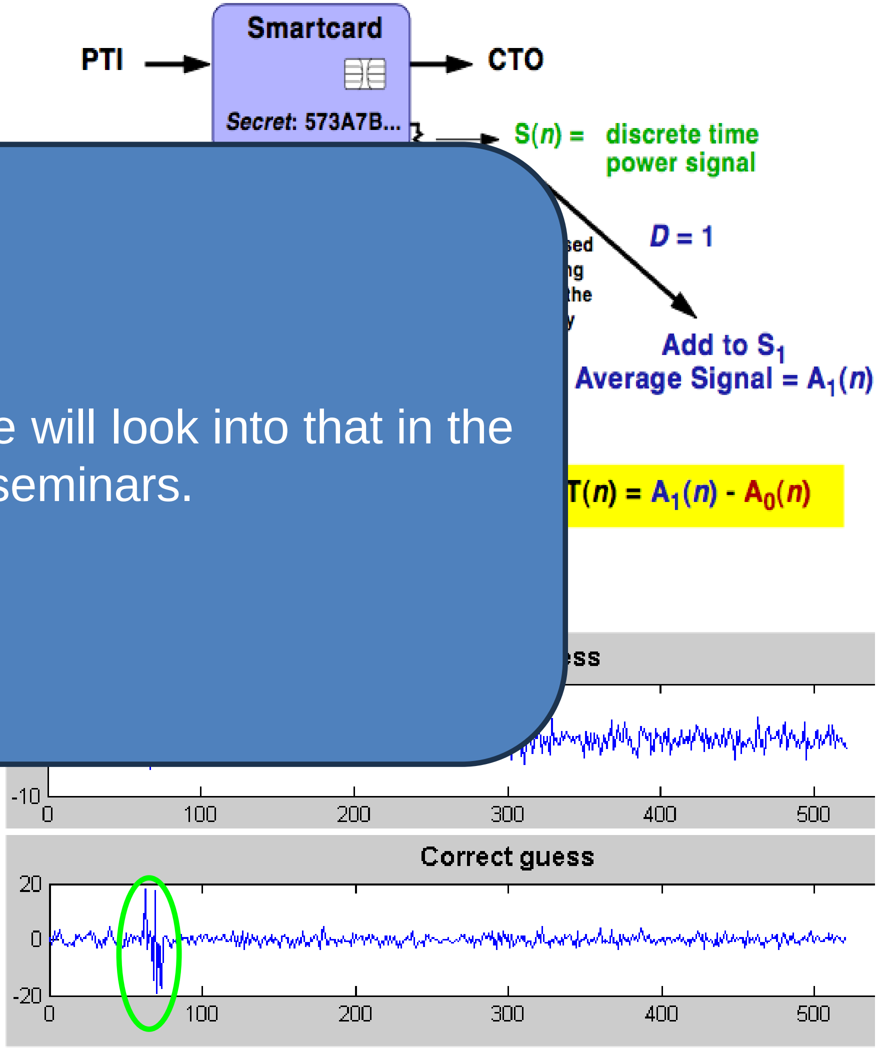
Differential power analysis

- Very Powerful attack on secret values (keys)
  - E.g., Sbox(KEY ⊕ INPUT_DATA)

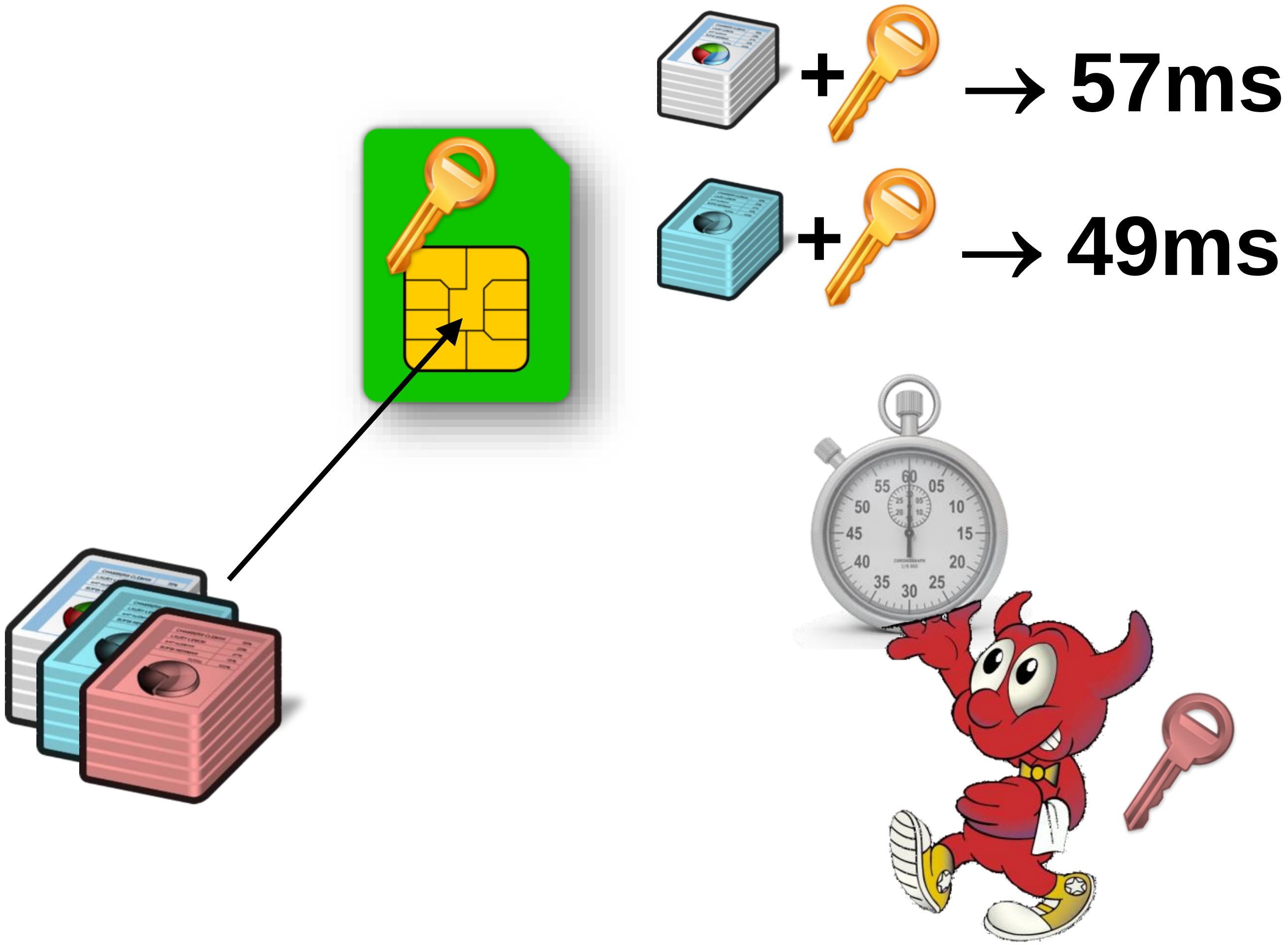
1. Obtain multiple power traces wit
   and variable data
   - 10^3-10^6 traces with known I/O d
   - Sbox(KEY ⊕ KNOWN_DATA)
2. Guess key byte-per-byte
   - All possible values of single byte
   - D = HammWeight(Sbox(KEY ⊕
   - Correct guess reveals correlatio
   - Incorrect guess not
3. Divide and test approach
   - Traces divided into 2 groups
   - Groups are averaged A_0 and A_1 (noise reduced)
   - Subtract group's averaged signals T(n)
   - Significant peaks if guess was correct

- No need for knowledge of exact implementation
  big advantage

This is important and we will look into that in the coming seminars.

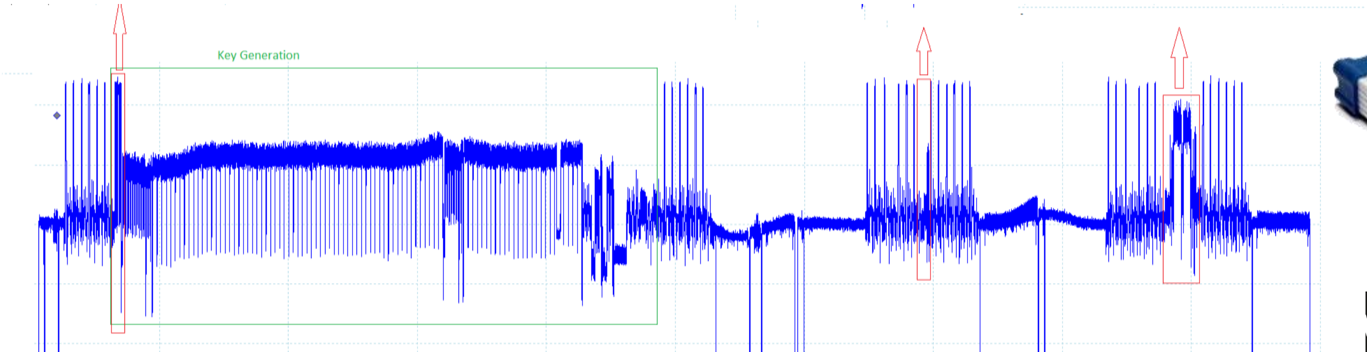


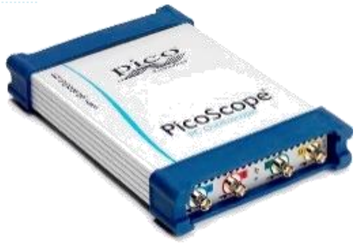
Timing attack: principle



Timing attacks

- Execution of crypto algorithm takes different time to process input data with some dependence on secret value (secret/private key, secret operations…)
  1. Due to performance optimizations (developer, compiler)
  2. Due to conditional statements (branching)
  3. Due to cache misses or other microarchitectural effects
  4. Due to operations taking different number of CPU cycles
- Measurement techniques
  1. Start/stop time (aggregated time, local/remote measurement)
  2. Power/EM trace (very precise if operation can be located)





Naïve modular exponentiation (modexp) (RSA/DH…)

- $M = C^d \bmod N$

Is there any dependency of time on secret value?

- $M = \overbrace{C * C * C * \ldots * C}^{\text{d-times}} \bmod N$

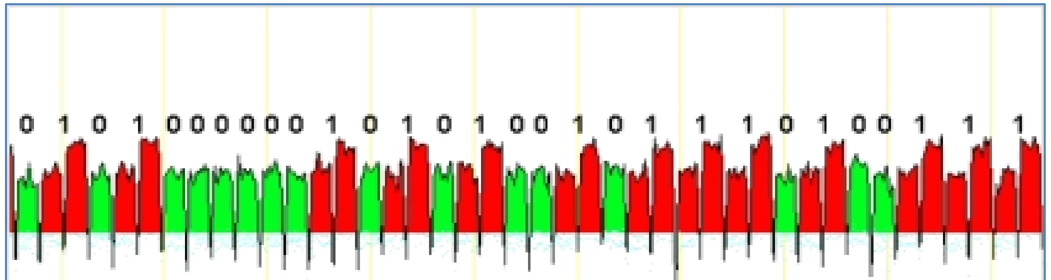
- Easy, but extremely slow for large d (e.g., >1000s bits for RSA)
  - – Faster algorithms exist

Faster modexp: Square and multiply algorithm

Executed always

Executed only when $d_j == 1$

```
// M = C^d mod N
// Square and multiply algorithm
x = C                         // start with ciphertext
for j = 1 to n {              // process all bits of private exponent
    x = x*x mod N             // shift to next bit by x * x (always)
    if (dj == 1) {            // j-th bit of private exponent d
        x = x*C mod N         // if 1 then multiple by Ciphertext
    }
}
return x        // plaintext M
```



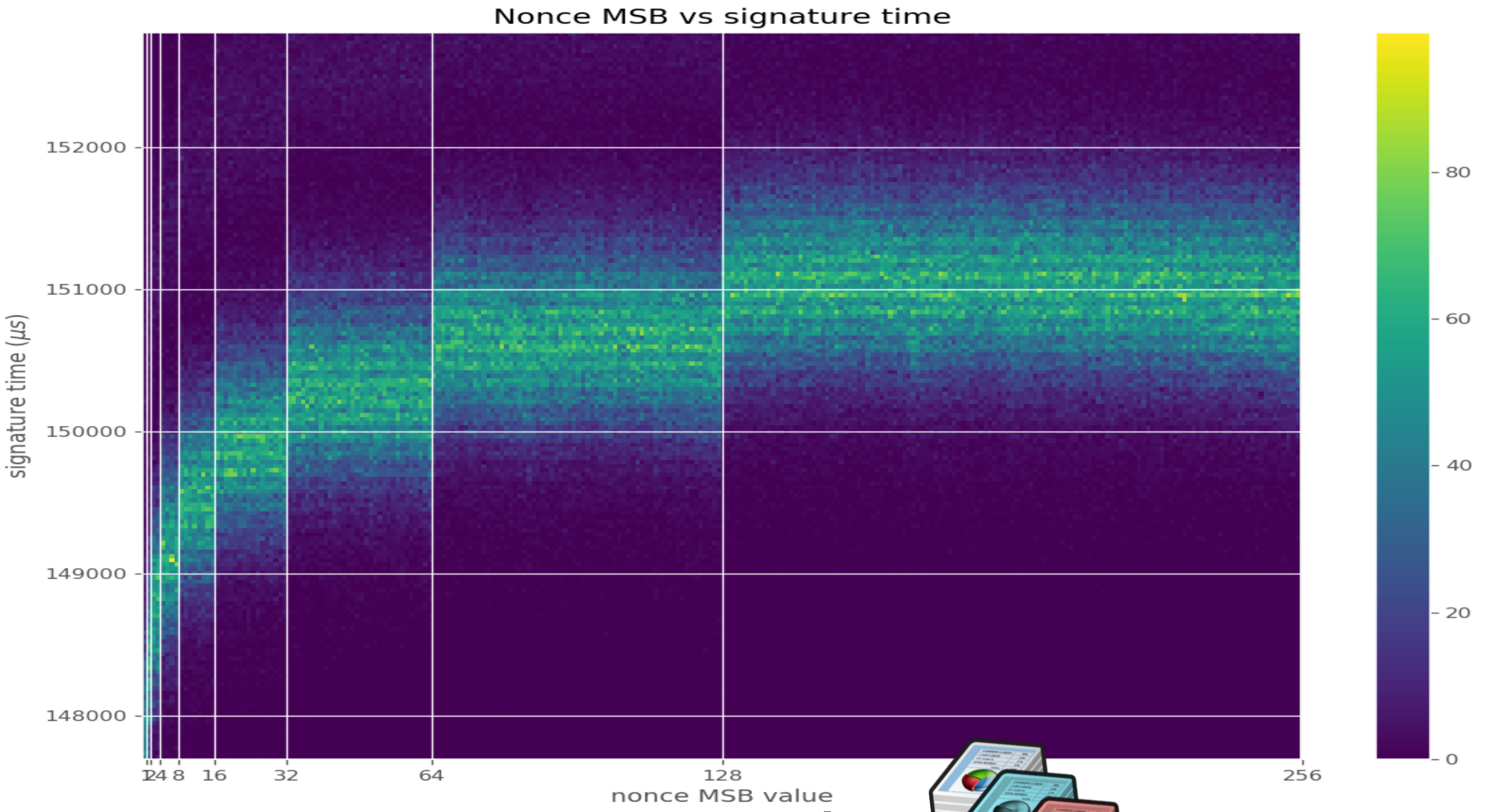
Gilbert Goodwill, http://www.embedded.com/print/4408435 (dead link)

- How to measure?
  - Exact detection from simple power trace
  - Extraction from overall time of multiple measurements

Gather data → Analyse → Bias found → Impact

Run ECC operations → MSB/time → Bias found in ECDSA → CVE-2019-15809

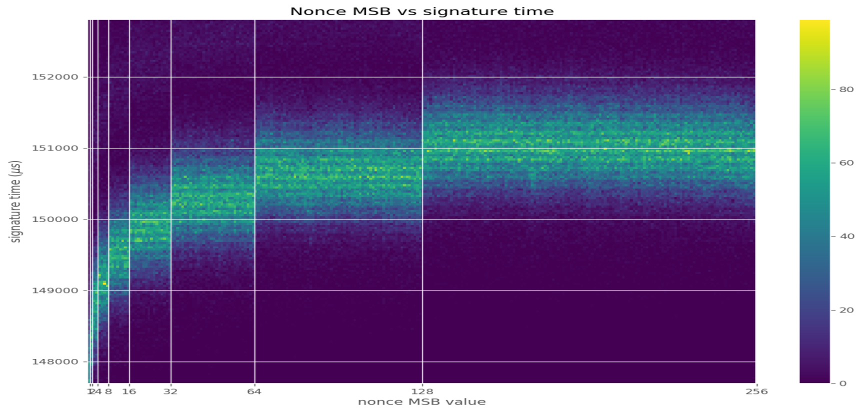
Signature time (µs)



Nonce MSB value

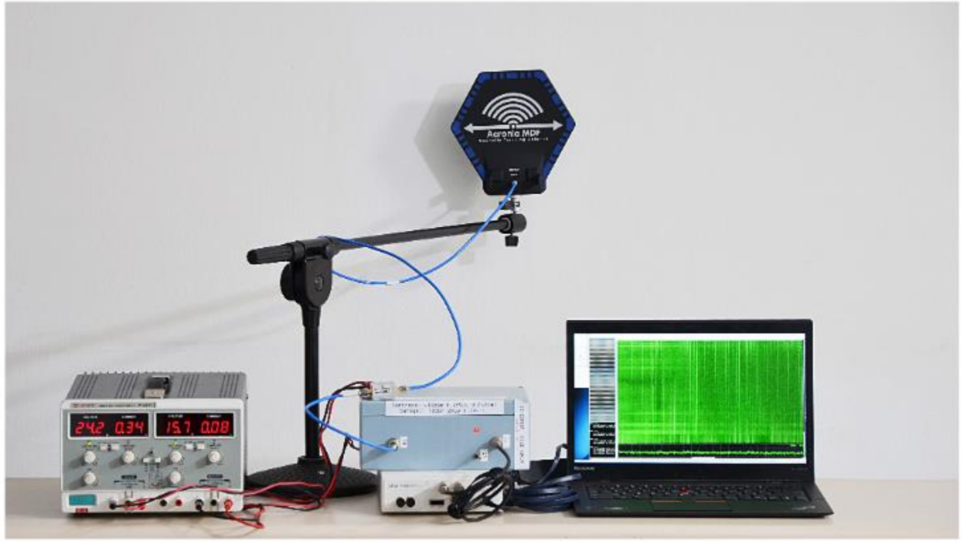
Minerva vulnerability CVE-2019-15809 (10/2019)

- Discovered by ECTester (https://github.com/crocs-muni/ECTester)
- Athena IDProtect smartcard (CC EAL 4+)
  - FIPS140-2 #1711, ANSSI-CC-2012/23
  - Inside Secure AT90SC28872 Microcontroller
  - (possibly also SafeNet eToken 4300…)
- Libgcrypt, wolfSSL, MatrixSSL, Crypto++
- SunEC/OpenJDK/Oracle JDK
- Small time difference leaking few top bits of nonce
- Enough to extract whole ECC private key in 20-30 min
  - ~thousands of signatures + lattice-based attack

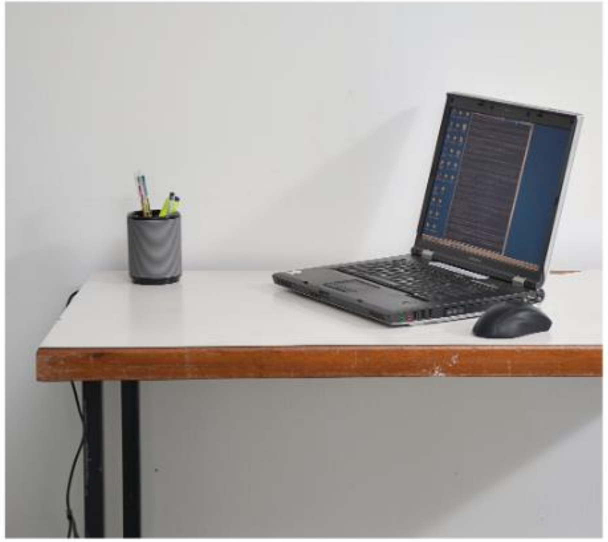


Example: Practical TEMPEST for $3000

- ECDH Key-Extraction via Low-Bandwidth Electromagnetic Attacks on PCs
  - https://eprint.iacr.org/2016/129.pdf
- E-M trace captured (across a wall)



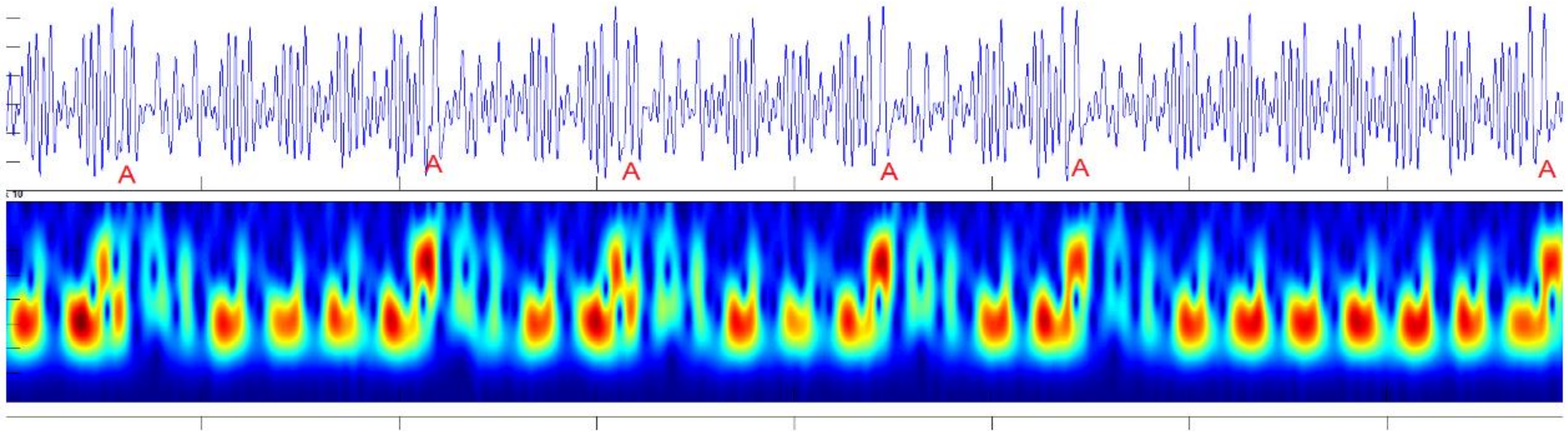
(a) Attacker's setup for capturing EM emanations. Left to right: power supply, antenna on a stand, amplifiers, software defined radio (white box), analysis computer.



(b) Target (Lenovo 3000 N200), performing ECDH decryption operations, on the other side of the wall.

Example: Practical TEMPEST for $3000

- ECDH implemented in latest GnuPG's Libgcrypt
- Single chosen ciphertext – used operands directly visible



Example: How to evaluate attack severity?

- What was the cost?
  - Not particularly high: $3000
- What was the targeted implementation?
  - Widely used implementation: latest GnuPG's Libgcrypt
- What were preconditions?
  - Local physical presence, but behind the wall
- Is it possible to mitigate the attack?
  - Yes: fix in library, physical shielding of device, perimeter…
  - What is the cost of mitigation?

Other types of side-channel attacks

- Acoustic emanation
  - Keyboard clicks, capacitor noise
  - Speech eavesdropping based on high-speed camera
- Cache-occupation side-channel
  - Cache miss has impact on duration of operation
  - Other process can measure own cache hits/misses if cache is shared
  - https://github.com/defuse/flush-reload-attacks
  - http://software.imdea.org/projects/cacheaudit/
- Branch prediction side-channel (Meltdown, Spectre)
  - (separate short course running now)

MITIGATIONS

Generic protection techniques

1. Do not leak
   - Constant-time crypto, bitslicing…
2. Shielding - preventing leakage outside
   - Acoustic shielding, noisy environment
3. Creating additional “noise”
   - Parallel software load, noisy power consumption circuits
4. Compensating for leakage
   - Perform inverse computation/storage
5. Prevent leaking exploitability
   - Ciphertext and key blinding, key regeneration, masking of the operations

Example: NaCl (“salt”) library

libsodium

- Relatively new cryptographic library (2012)
  - Designed for usable security and side-channel resistance (mostly time!)
  - D. Bernstein, T. Lange, P. Schwabe
  - https://cr.yp.to/highspeed/coolnacl-20120725.pdf
  - Actively developed fork is libsodium https://github.com/jedisct1/libsodium
    - Also check μNaCl for embedded devices: https://munacl.cryptojedi.org/
- Designed for usable security (hard to misuse)
  - Fixed selection of good algorithms (AE: Poly1305, Sign: EC Curve25519)
  - `c = crypto_box(m,n,pk,sk), m = crypto_box_open(c,n,pk,sk)`
- Implemented to have constant-time execution
  - No data flow from secrets to load addresses
  - No data flow from secrets to branch conditions
  - No padding oracles (recall CBC padding oracle in PA193)
  - Centralizing randomness and avoiding unnecessary randomness
- Extra side-channel and fault injection protections: https://github.com/sca-secure-library-sca25519/sca25519

How to test real implementation?

1. Be aware of various side-channels
2. Obtain measurement for given side-channel
   - Many times (10^3 - 10^7), compute statistics; is it enough?
   - Same input data and key; group A
   - Same key and different data; group B
   - Different keys and same data…
3. Compare groups of measured data
   - Is difference visible? => potential leakage
   - Is distribution uniform? Is distribution normal?
   - More advanced methods, for example: Test Vector Leakage Assessment:
     - https://docplayer.net/45501976-Test-vector-leakage-assessment-tvla-methodology-in-practice.html
4. Try to measure again with better precision ☺

Active Side-Channel

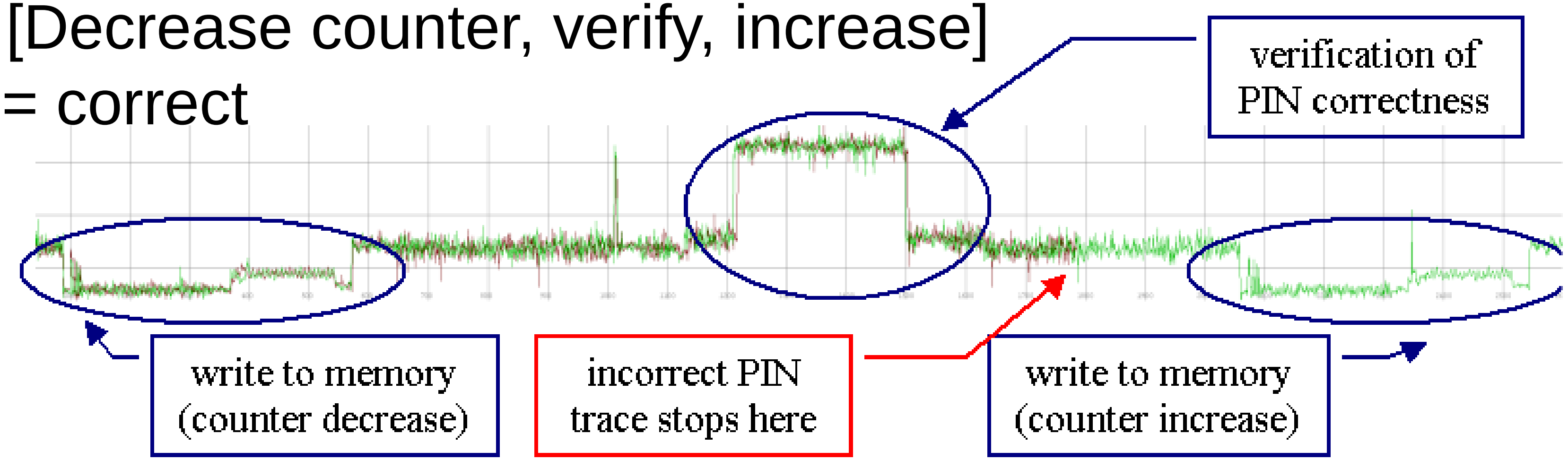
FAULT INJECTION ATTACKS

Semi-invasive attacks

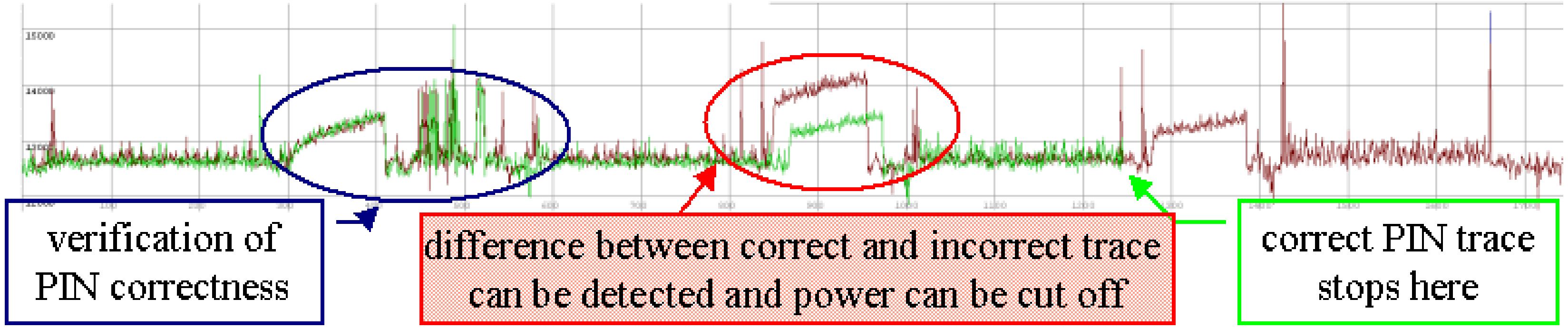
- “Physical” manipulation (but card still working)
- Micro probes placed on the bus
  - After removing epoxy layer
- Fault induction
  - liquid nitrogen, power glitches, light flashes…
  - modify memory (RAM, EEPROM), e.g., PIN counter
  - modify instruction, e.g., conditional jump

PIN verification procedure

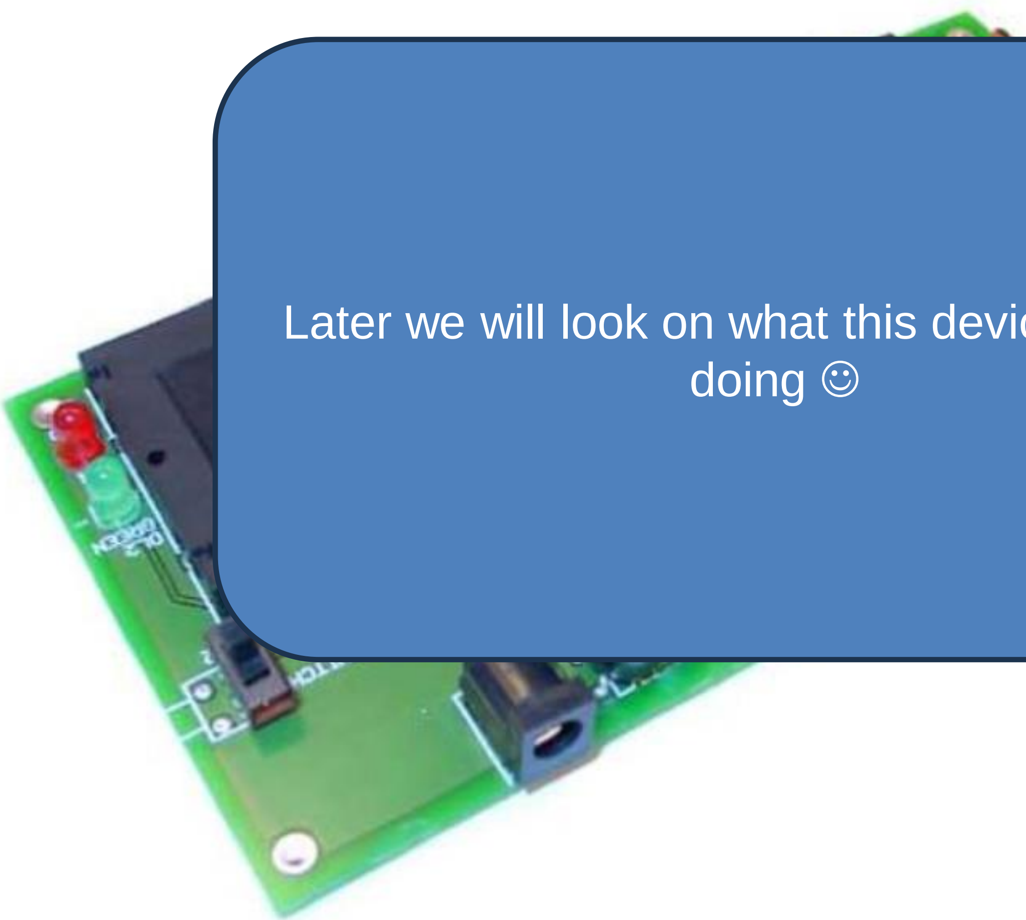
- [Decrease counter, verify, increase] = correct



- [Verify, decrease/increase]



FI Example: the “unlooper” device



Later we will look on what this device might be doing ☺

Conclusions

- Trusted element is secure anchor in a system
  - Understand why it is trusted and for whom
- Trusted element can be attacked
  - Non-invasive, semi-invasive, invasive methods
- Side-channel attacks are very powerful techniques
  - Attacks against particular implementation of algorithm
  - Attack possible even when algorithm is secure (e.g., AES)
- Use well-know libraries instead own implementation

What will be looking at?