MUNI
FI

PV191: Introduction

Course organization, introduction to HDL tools

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Course Organization

- Silicon design group
  - A415, Thursday 12:00 – 14:00
  - Group projects
  - Consultations
- Tiny Tapeout
  - https://tinytapeout.com/
  - TT06: 19.04.2024

Tiny Tapeout Possibilities

- Pins:
  - clk
  - rst
  - 8x inout
  - 8x out
  - 8x in
- Limitations:
  - Output max. frequency 33 MHz
  - Input max. frequency 66 MHz

Tiny Tapeout Flow

- Watch how to started video

- Fork example Github project
  - https://github.com/TinyTapeout/tt06-verilog-template
  - Allow github action: Settings -> Pages -> Build and deployment -> Source -> Github actions
  - Modify info.yaml with your project information
- Make changes and push to github

Tiny Tapeout Design Ideas

- Inspire yourself by previous projects:
  - https://tinytapeout.com/runs/
- Community ideas:
  - https://docs.google.com/document/d/1EtuYTrtAT3-umwonZHsstT9JR8zM2rreEYxW4RXH98o/edit#heading=h.8ghyyq6b1smo