



# ON Semiconductor

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**Přednáška předmětu F5900 Fyzika ve firmě, 2017**

**Přírodovědecká fakulta Masarykovy univerzity**

**Michal Lorenc, [michal.lorenc@onsemi.com](mailto:michal.lorenc@onsemi.com)**



# Obsah

Úvod

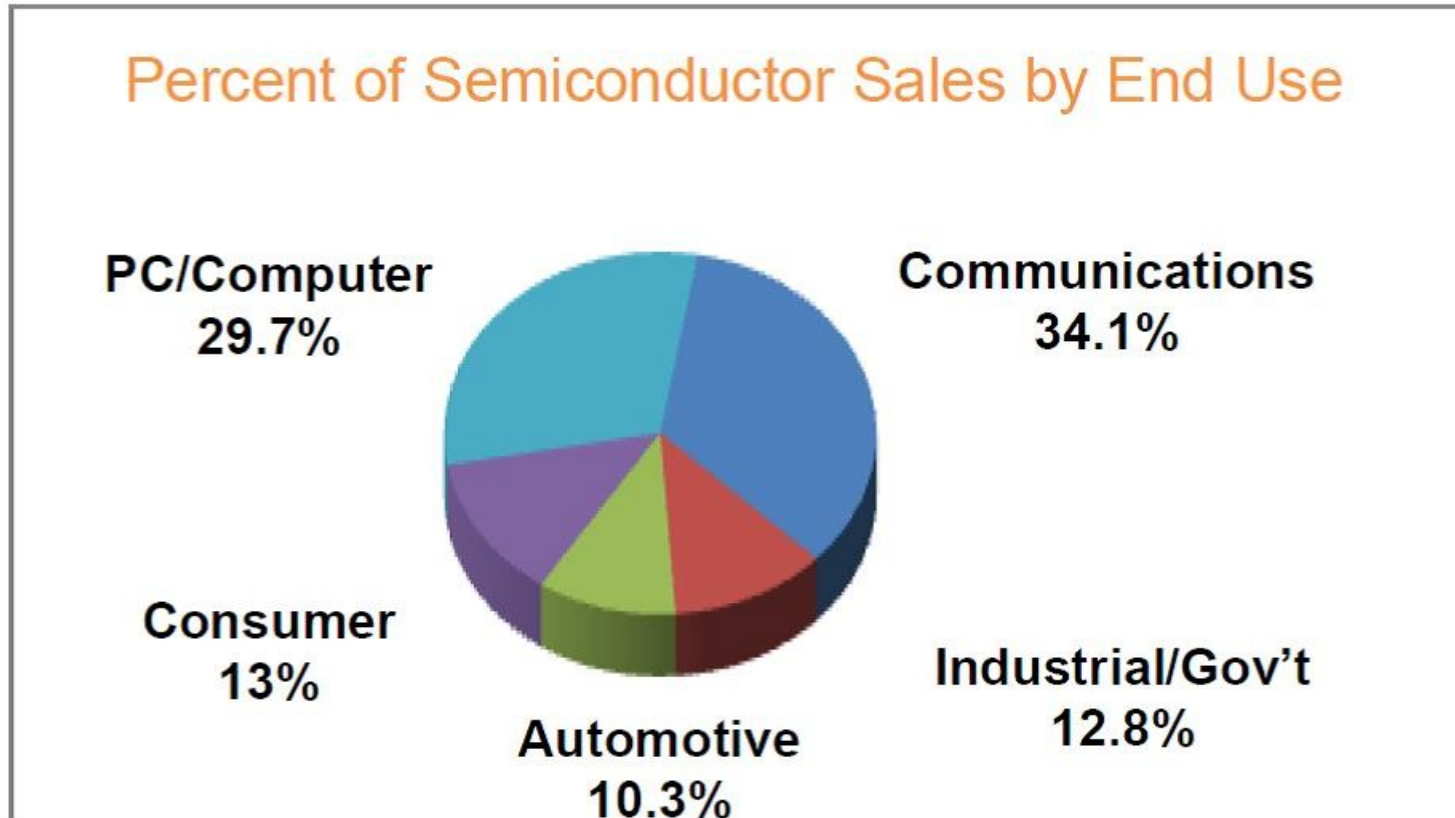
Polovodičový průmysl, ON Semiconductor

Uplatnění

Polovodičová technologie a fyzika

- Růst krystalů
- Procesy výroby desek
- SOI, GaN, SiC
- Analýzy a měření
- Výpočty a simulace

# 2015 Global Semiconductor Market: \$335 Billion



Source: WSTS End Use Report, 2015

Note: Military is <1% and is included in Industrial/Gov't

<b>Total Semiconductors - \$335.2B</b>						
<b>Integrated Circuits - \$274.5B</b>					<b>Discretes Sensors &amp; Opto \$60.7B</b>	
<b>Digital - \$229.3B</b>				<b>Analog \$45.2B</b>		<b>Discretes \$18.6B</b>
<b>MOS - \$229.3B</b>				<b>General Purpose \$18.6B</b>	<b>App. Specific \$26.6B</b>	
<b>Memory - \$77.2B</b>		<b>Micro - \$61.3B</b>		<b>Logic - \$90.8B</b>		
<b>DRAM \$45.0B</b>	<b>Flash \$30.4B</b>	<b>MPU \$43.3B</b>	<b>MCU \$15.5B</b>	<b>Special Purpose Logic \$70.2B</b>	<b>Standard Logic \$20.6B</b>	

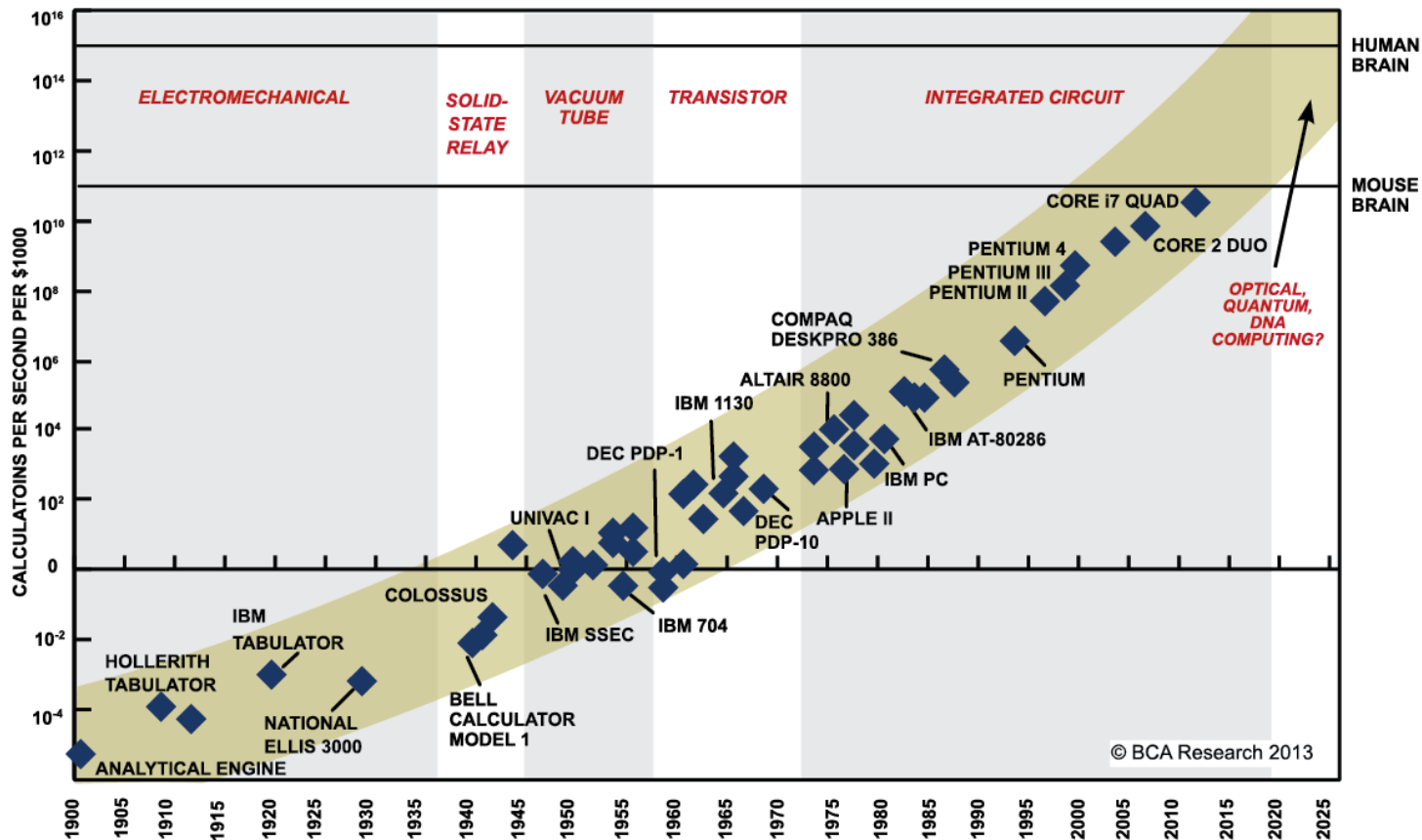
Sensors \$8.8B

Note: Numbers are rounded  
Source: WSTS

SRAM \$0.4B  
Non-volatile memory; ROMs; EPROM; EEPROM \$1.4B  
DSP \$2.5B



# Moorův zákon



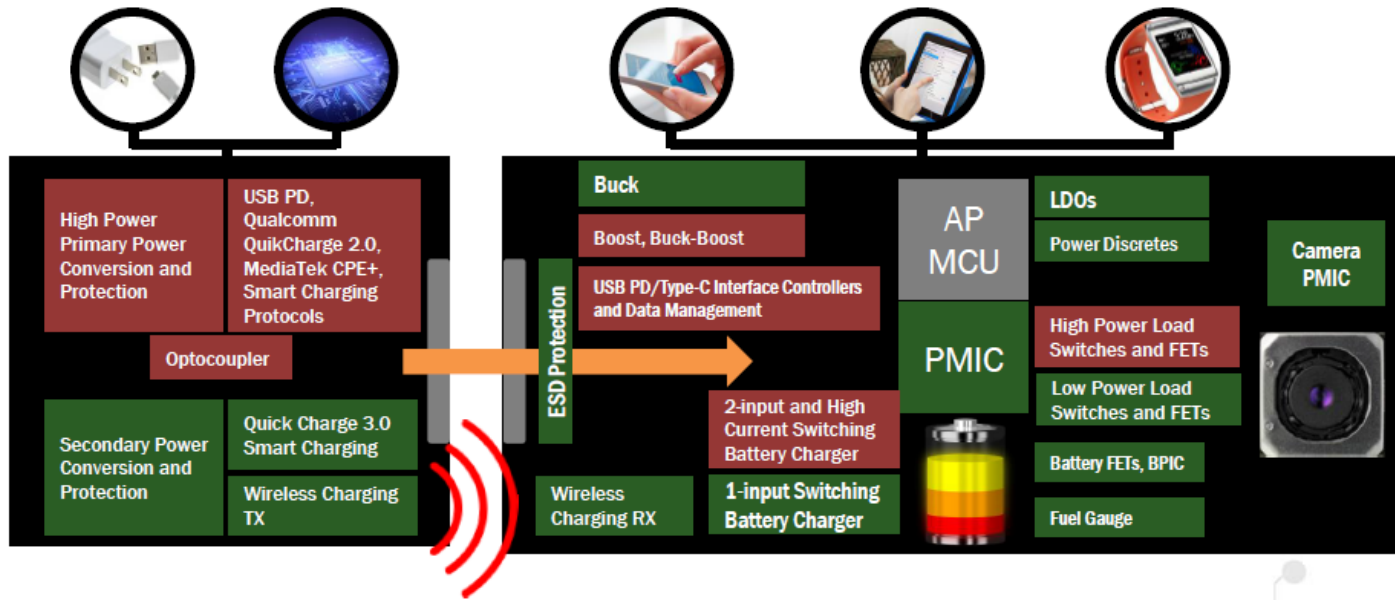
SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, THE VIKING PRESS, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

- ... počet tranzistorů na stejné ploše čipu se každé dva roky zdvojnásobí
- min. rozměr tranzistoru: 5 nm? (odhad z 1961 – 10 μm, 2000 – 16 nm)
- dnes: 12 nm

# RETHINK ENERGY EFFICIENCY.



# ADDRESSABLE CONTENT OF \$9 IN SMARTPHONES



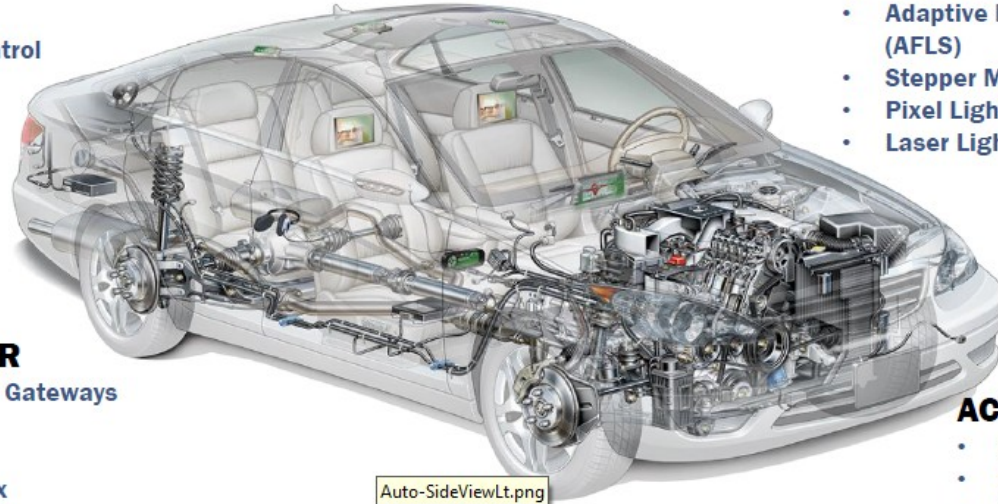
# ADDRESSABLE CONTENT OF \$200-\$400<sup>1</sup> IN AUTOS

## POWERTRAIN

- Engine Control
- Transmission Control
- Ignition
- Throttle Control
- Start-Stop
- 48 V System
- Electrification
- Charging

## BODY & INTERIOR

- Body Computers & Gateways
- HVAC
- Door & Seat
- Smart-Junction Box
- Instrument Clusters
- Infotainment
- Connectivity
- Wireless Charging



## IN-VEHICLE NETWORKING

- LIN/CAN, SBC, FlexRay & Ethernet

## LIGHTING

- LED Exterior
- LED Interior
- Adaptive Front Lighting System (AFLS)
- Stepper Motor Control
- Pixel Lighting
- Laser Lighting

## ACTIVE SAFETY

- Rear View Camera
- Surround View Camera
- Park Assist
- Forward-Looking ADAS
- In-Cabin ADAS
- E-Mirror

ON Semiconductor®





# A LEADER IN VEHICLE ELECTRIFICATION

## ON-BOARD CHARGER

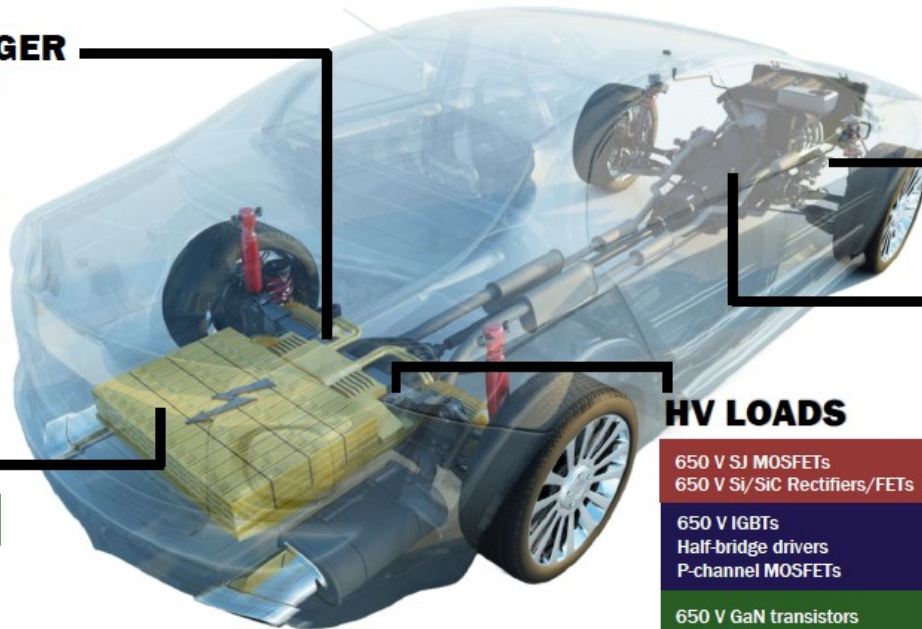
650 V SJ MOSFETs  
650 V Si/SiC Rectifiers/FETs  
Automotive HV modules  
Gate drivers

650 V IGBTs

650 V GaN transistors  
Op-amps & current sense  
DC-DC, LDO, IVN, ASIC

## BATTERY MANAGEMENT

40 V FETs (lowest RDS(on))



## MAIN DRIVE

650/1200 V Rectifiers  
1200 V SiC Rectifiers/FETs

650/1200 V IGBTs

650 V GaN transistors  
Op-amps & current sense  
DC-DC, LDO, IVN, ASIC

## 12V 48V DC-DC

80/100 V FETs  
Half-bridge drivers (high speed)

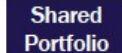
40 V FETs  
Op-amps & current sense  
DC-DC, LDO, IVN, ASICs

## HV LOADS

650 V SJ MOSFETs  
650 V Si/SiC Rectifiers/FETs

650 V IGBTs  
Half-bridge drivers  
P-channel MOSFETs

650 V GaN transistors  
Automotive modules  
Op-amps & current sense  
DC-DC, LDO, IVN, ASICs

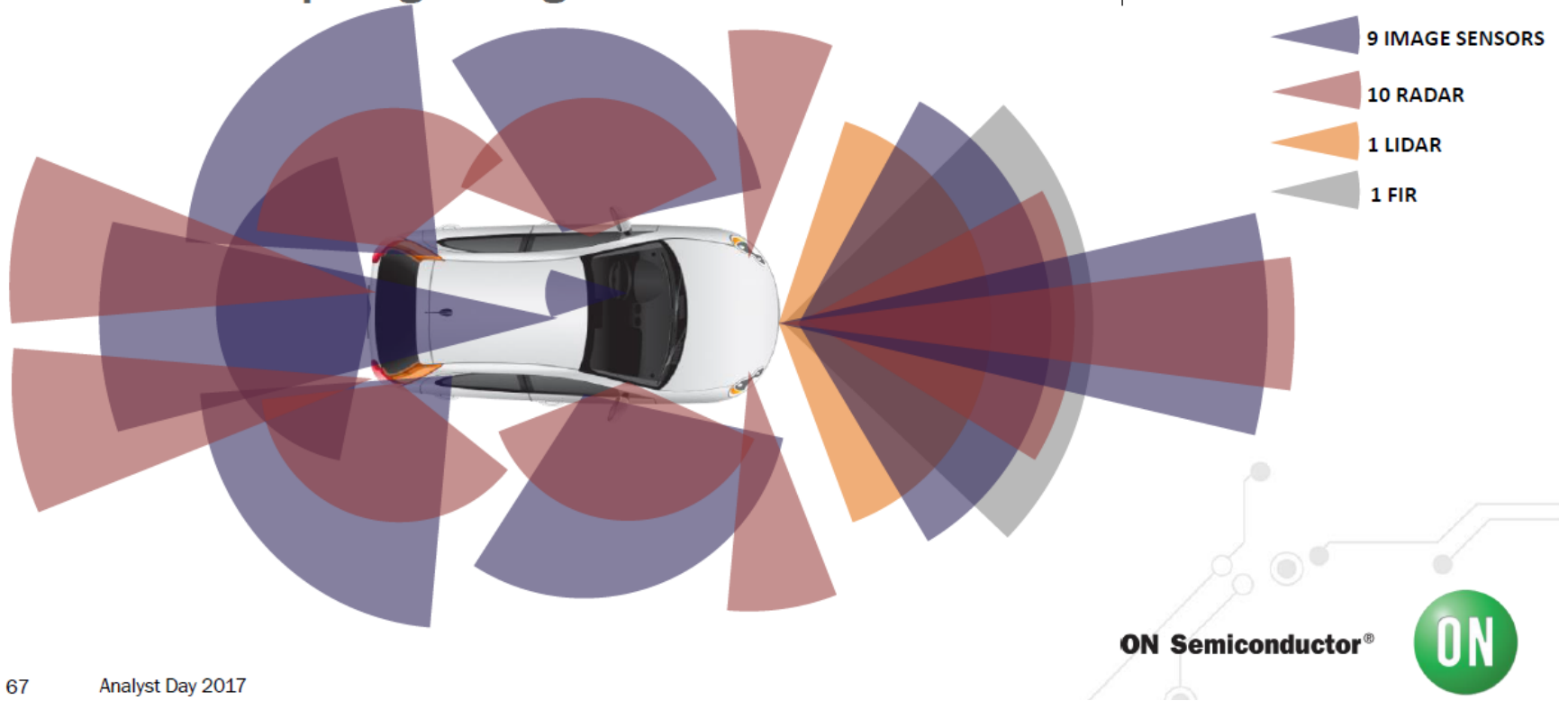


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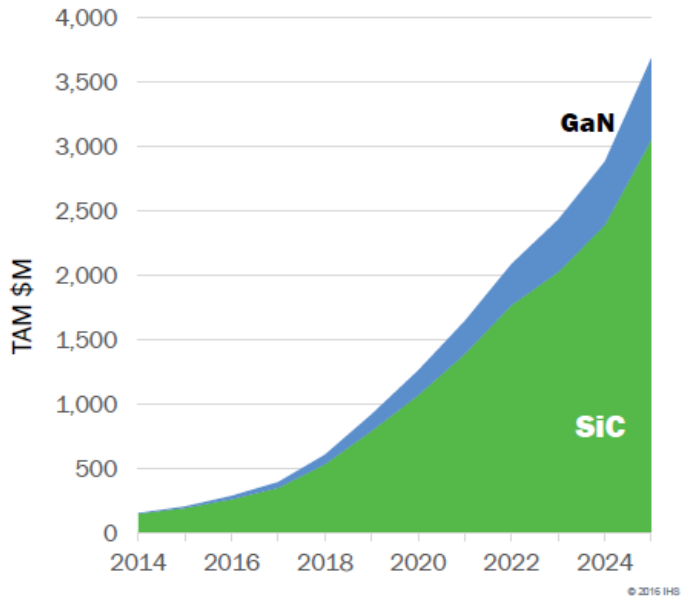
# IMAGING + RADAR FUSION

Customers Requiring 9 Imagers and 10 Radar Transceivers



67 Analyst Day 2017

# PSG GaN AND SiC PROGRAMS



**Currently producing and sampling all SiC & GaN power technologies**

## KEY SiC & GaN BENEFITS

- Power Supplies: smaller form factor
- Automotive EV: no liquid cooling → reduced weight
- Auto On Board Charging: faster charge time
- Solar Energy: higher power efficiency



**ON Semiconductor®**



# ON Semiconductor - úvod

Headquarters: **Phoenix**, Arizona

Employees: **29 thousand** worldwide

## Manufacturing:

Belgium

Canada

China

Czech Republic

Japan

Korea

Malaysia

Philippines

Republic of Korea

United States

Vietnam

## Design Centers:

Belgium

Canada

Czech Republic

France

Germany

India

Ireland

Japan

Korea

Philippines

Romania

Slovak Republic

Switzerland

Taiwan

United States

## Solution Engineering Centers:

China, Shanghai

China, Shenzhen

Germany, Munich

Japan, Tokyo

Korea, Seoul

Taiwan, Taipei

United States, Detroit

United States, Portland

United States, San Jose

## Revenue:

2015 \$3.496 bil.

2016 \$3.906 bil.

2017 \$5 bil.

**ON Semiconductor (Nasdaq: ON)** is driving energy efficient innovations, empowering customers to reduce global energy use.

The company is a leading supplier of semiconductor-based solutions, offering a comprehensive portfolio of energy efficient connectivity, sensing, power management, analog, logic, timing, discrete, and custom devices.

The company's products help engineers solve their unique design challenges in automotive, communications, computing, consumer, industrial, medical and military/aerospace applications.



# TESLA Rožnov - historie

**1957** - Vyroben první Ge tranzistor.

Svět: 1947 (1951+)

**1961** - Vyroben první Si tranzistor.

1962 - Vyroben první barevná obrazovka.

**1967** - Vyroben první integrovaný obvod.

Svět: 1959

1989 - **TESLA** Rožnov je státním podnikem s 8500 zaměstnanci a vyrábí barevné televizní obrazovky, polovodičové materiály a součástky a mnoho dalších zařízení.

1992 - Rozdělením státního podniku na 16 menších celků vzniká společnost **TESLA SEZAM** (výroba čipů) a **TEROSIL** (výroba křemíku).

1993 - Počátky spolupráce se strategickým partnerem - společností **MOTOROLA**. Založeno návrhové středisko v Rožnově - SCG Czech Design Center.

1996 – Dosažena výrobní kapacita 2000 desek (průměru 100 mm) s čipy za týden.

1997 - Konec privatizačního procesu, **MOTOROLA** se stává akcionářem společností **TESLA SEZAM** a **TEROSIL**.

# ON SEMICONDUCTOR CZECH REPUBLIC

2003 - TEROSIL + TESLA SEZAM = **ON SEMICONDUCTOR CZECH REPUBLIC.**

2005 - ON Semiconductor (NASDAQ: ON) se stává 100% vlastníkem.

2007 - Výroba prvního krystalu průměru 8“.

2008 - Akvizice AMI Semiconductor - návrhové středisko AMIS Brno.

- Konverze z desek průměru 100 mm na 150 mm.

2013 - Expanze výroby křemíkových desek průměrů 125, 150 a 200 mm.

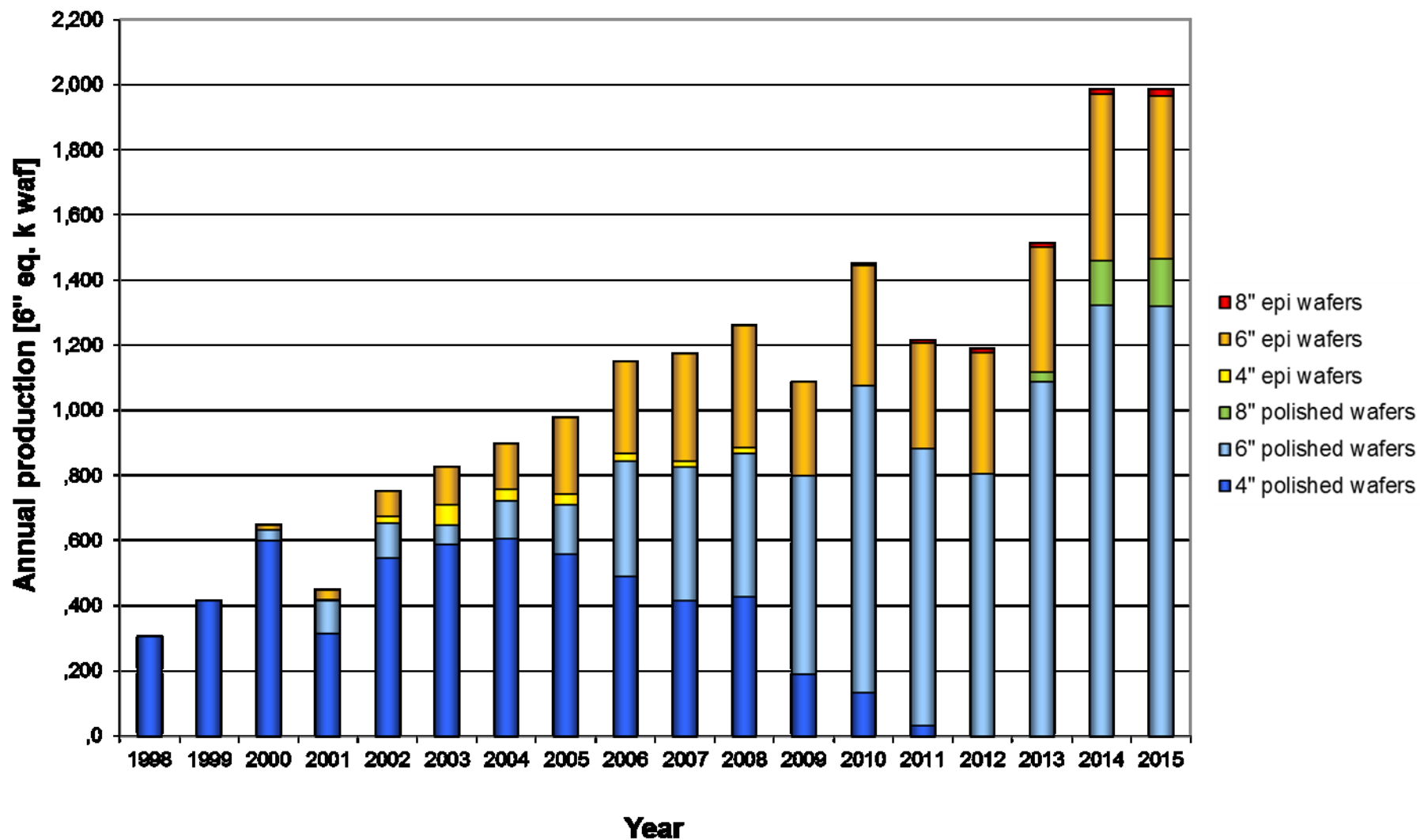
2014 - Zahájení VaV MOCVD technologie pro epitaxní růst struktur Ga(Al)N na Si.

2016 - Kvalifikace SOI technologie (Silicon-On-Insulator).

2017 - Zahájen VaV SiC technologe.

- Expanzní projekty pro podstatné zvýšení kapacit výroby.

# Výroba Si desek v Rožnově



# Uplatnění fyziky (konkrétní pracovní pozice)

## Výzkum a vývoj

- Material Science Engineer
- R&D Device Engineer
- R&D Integration Engineer

## Vývoj nových produktů

## Technologie (Engineering)

- Výrobní technologie (Technolog operace)
- Měření

## Výroba

- Směnový technolog
- Technik údržby

## Podpůrné úseky

## Management a project management



- ▶ Struktura společnosti
- společnosti
- ▶ Pro zájemce o práci
- ▶ Pro studenty
- Kontakty
- ▶ Pro tisk a veřejnost

Home > Česká republika

## POMÁHÁME VE VÝZKUMU VESMÍRU

Náš pixelový detektor pro projekt ATLAS - CERN



### Volná místa

#### ROŽNOV POD RADHOŠTĚM

##### ENGINEERING

- » TEST ENGINEER / Test inženýr
- » APPLICATION ENGINEER / Vývojový inženýr elektro

- » VÝVOJÁŘ - ELEKTRONIK
- » PRODUCT ENGINEER
- » DESIGN ENGINEER / Konstruktor elektro

##### IT

- » IT TESTER
- » SOFTWARE DEVELOPER
- » Jr. DBA ADMINISTRATOR

##### OSTATNÍ

- » ACCOUNTANT (fixed assets/travel) - ÚČETNÍ

##### PRODUCTION

- » PRODUKT INŽENÝR VÝROBY KŘEMÍKU
- » OPERÁTOR VÝROBY - PŘISPÍVÁME NA DOPRAVU
- » TECHNOLOG VÝROBY POLOVODIČŮ
- » TECHNIK PROVOZU VÝROBNÍCH FACILITIES
- » MATERIAL SCIENCE ENGINEER
- » TECHNIK PODPORY TESTOVÁNÍ

#### BRNO

##### ENGINEERING

- » DIGITAL DESIGN ENGINEER
- » MEMORY TEST ENGINEER
- » ANALOG & MIXED SIGNAL DESIGN ENGINEER

##### IT

- » LINUX ADMINISTRATOR

#### SLOVENSKO

##### ENGINEERING

- » DEVICE AND PRODUCT RELIABILITY ENGINEER / Inženýr kvality

### Aktuality

**NOVINKA PRO STUDENTY: Motivační stáže v zahraničí (24.3.2017)**

**Prohlídky ve výrobě (1.3.2017)**

**Učební pomůcky do škol (24.2.2017)**

**Exkurze pro studenty v roce 2016 (6.1.2017)**

**Vánoční jarmark neziskových organizací (19.12.2016)**

**Společnost ON Semiconductor vybavila elektronickou laboratoř pro středoškolské studenty (15.11.2016)**

**Plánované cvičení na stanici HCI v ON Semiconductor (10.10.2016)**

**Technický talent města Rožnova (7.10.2016)**

**Technický jarmark 2016 (7.10.2016)**

# Výzkumně - vývojové projekty

## Projekty řešené s podporou Technologické agentury ČR:

TA01010078: Struktury SOI pro pokročilé polovodičové aplikace (2011-2013)

TE01020233: Platforma pokročilých mikroskopických a spektroskopických technik pro nano a mikrotechnologie (2012-2019)

TH01011284: Nové polovodičové materiály a součástky s velkou šířkou zakázaného pásu

TH01010419: Výzkum a vývoj nových technologií výroby bipolárního tranzistoru s izolovaným hradlem (TIGBT)

TH02010014: Nové polovodičové struktury pro pokročilé elektronické aplikace

## Projekty řešené s podporou Ministerstva průmyslu a obchodu

FF-P/129: Vývoj polovodičových detektorů ionizujícího záření

FI-IM2/131: Výzkum a vývoj pokročilé křemíkové desky pro sub-mikronové technologie

FI-IM2/166: Výzkum a vývoj technologie pro výrobu detektorů záření na 150 mm křemíkových substrátech

FR-TI1/582: Výzkum a vývoj pokročilé komplementární bipolární technologie pro výrobu integrovaných obvodů

FR-TI3/031: Výzkum a vývoj technologií výroby nových typů křemíkových desek

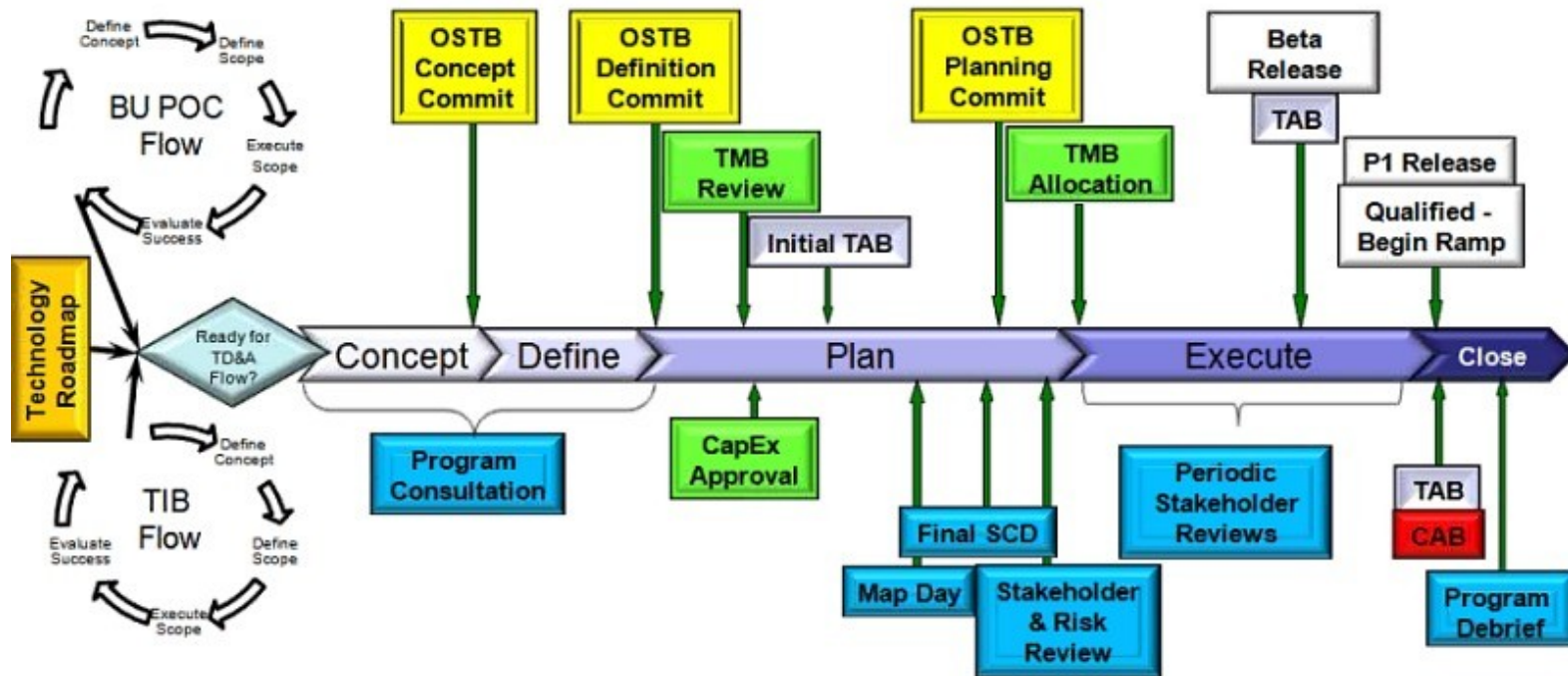
FR-TI3/534: Výzkum a vývoj pokročilých IGBT technologií pro vysokonapěťové výkonové aplikace

# Výzkumně - vývojové projekty

## Korporátní projekty:

- důsledně cílově orientované (nový produkt), 1 - 5 roků, rozpočet 100 k\$ - 10 mil.\$
- reporting na týdenní a měsíční bázi.

## Technology Development Process Timeline



# Výzkumně - vývojové projekty

## LDDA:

- od roku 2002 (PřF MU a FSI VUT)
- 4-6 projektů za rok
- financováno ON Semiconductor
- zapojení studentů

## IGA AMISPEC

- od roku 2013 (FSI VUT)
- 4-5 studentských projektů za rok
- financováno ON Semiconductor a TESCAN

## Jiné

- podpora investičních projektů korporace

# Stručná historie křemíku

Silicium, Silicon, Silizium, Sílicio, Kiesel, Kiesel, Кремний, Цахиур, Křemík, Kremík, , ケイ素

1787 A. Lavoisier – zkoumání křemene

1800 H. Davy – uvádí křemen jako sloučeninu

1811 L. J. Gay-Lussac, L. J. Thénard – příprava amorfního Si ( $\text{SiF}_4 + \text{K}$ )

1824 J. J. Berzelius – příprava amorfního křemíku  $\text{SiF}_4 + 4\text{K} \rightarrow 4\text{KF} + \text{Si}$  – objev nového prvku

1854 H. St. C. Deville – připravil krystalický Si (z  $\text{SiCl}_4 + \text{Al} \rightarrow \text{Si} + \text{AlCl}_3$ )

1907 N. Potter – reakcí uhlíku s křemenem připravil „čistý“ křemík

1916 J. Czochralski – vývoj nové metody růstu krystalů (kovů)

1946 J. Bardeen, W. Brattain, W. Shockley – polovodičový tým, vývoj tranzistoru

1948 G. K. Teal, J. B. Little – růst krystalů Ge a Si z kelímku

1951 H. E. Buckley – pojmenoval techniku tažení z kelímku po Czochralskim

1952 W. G. Pfann – „float zone melting“

1958 Výroba polykrystalického a následně monokrystalického Si v Rožnově

1959 W. Dash – využil zúžení zárodku krystalu pro zamezení šíření dislokací

1985 Czochralskiho metoda se stala dominantní technologií výroby mono Si

1992 vzniká TEROSIL – jeden z nástupců TESLY

1997 vstup MOTOROLY do TEROSILU

1999 TEROSIL/ ON SEMICONDUCTOR

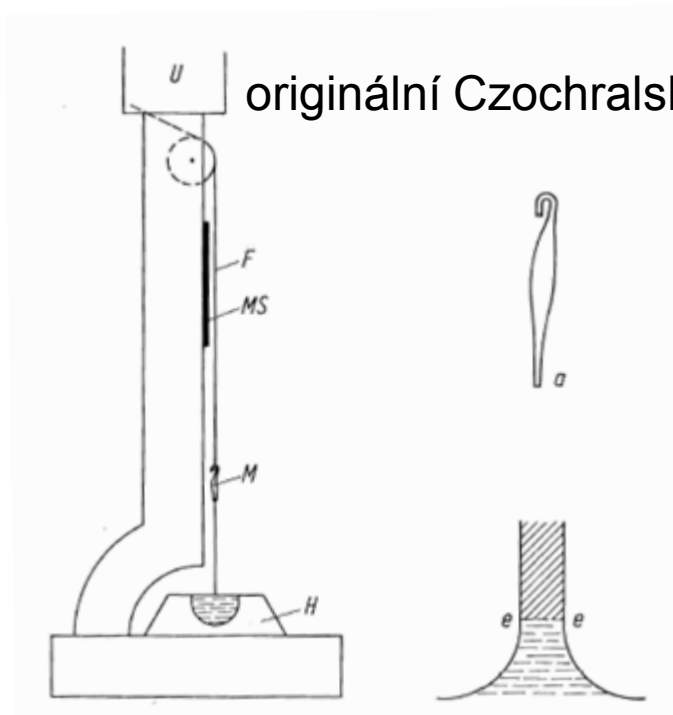
2003 ON SEMICONDUCTOR CZECH REPUBLIC

Sileacón, Shillagon, Sylycon, Silisiom, Silici, Siliciu, Silitsiumu, Krzem, Силицијум, Силиций, Silicijan

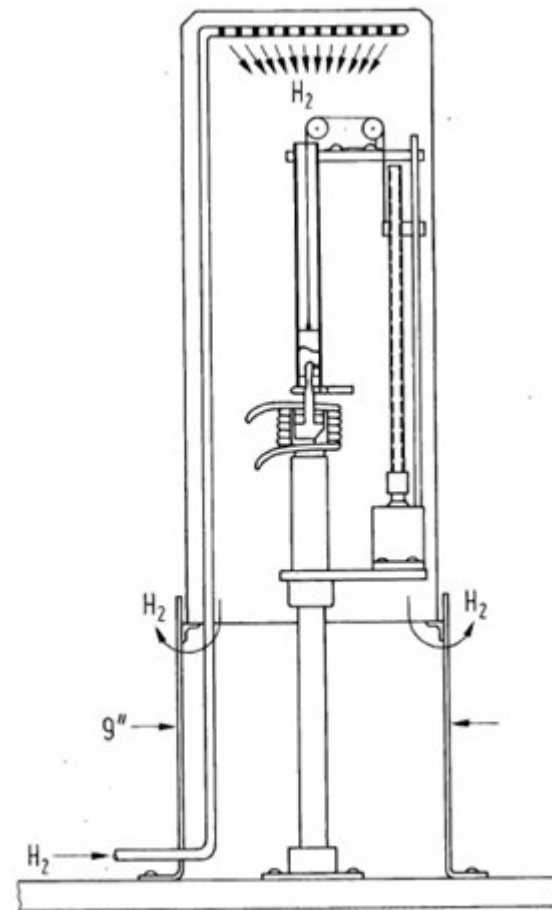
# První technologie výroby křemíku



krystalický Si - 1854 - H. St. C. Deville

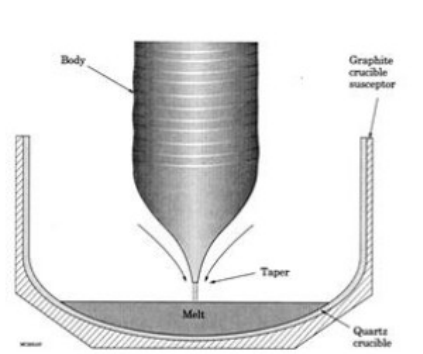
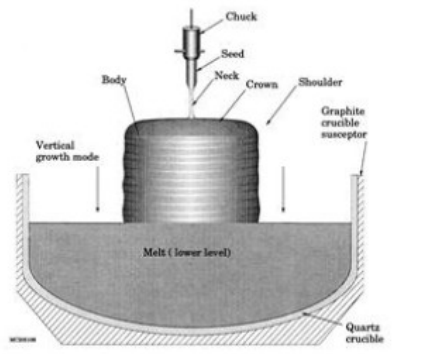
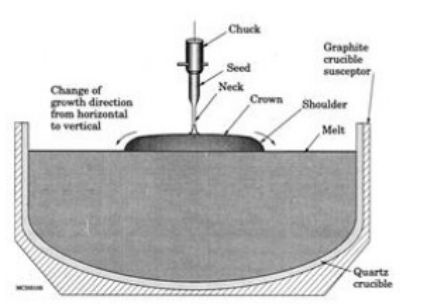
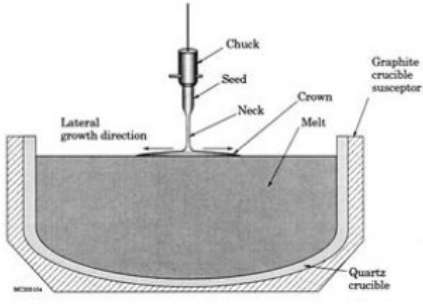
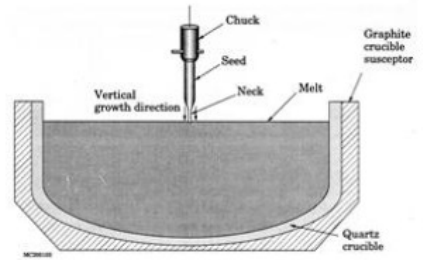
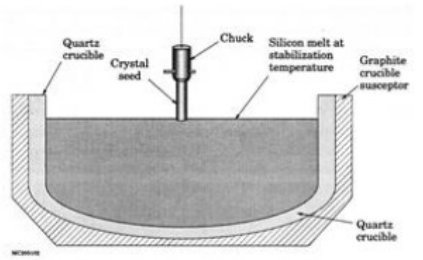
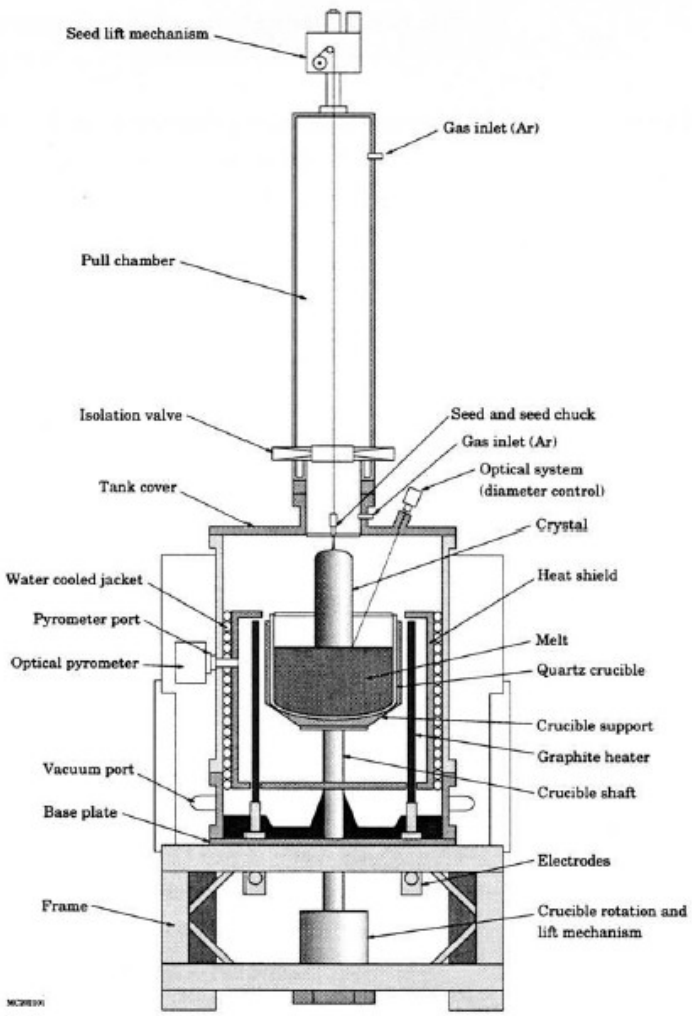


originální Czochralskiho aparatura - 1918

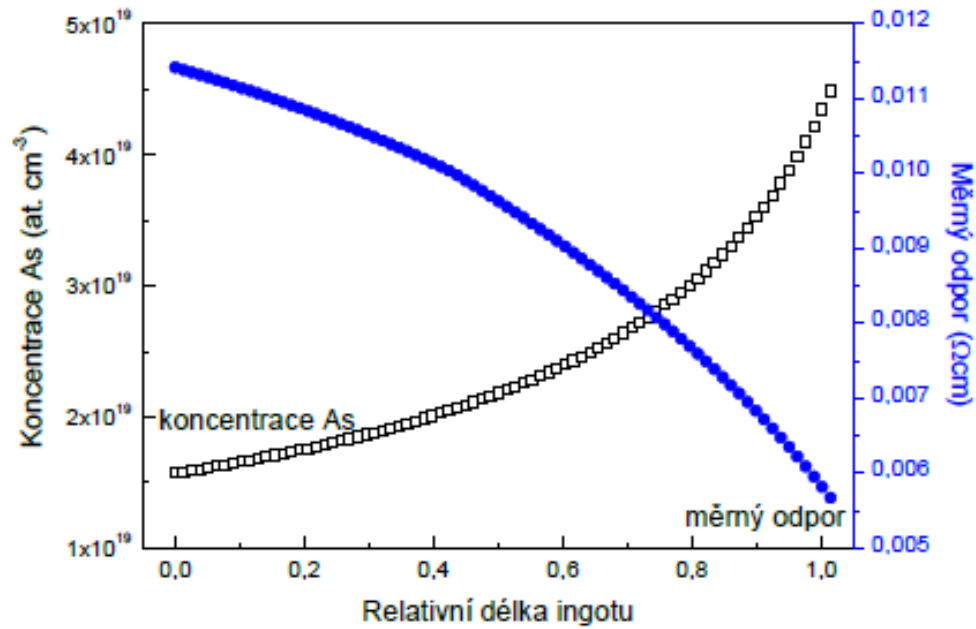


„Teal-Little“ aparatura - 1948

# Czochralskiho tažení krystalů z kelímku



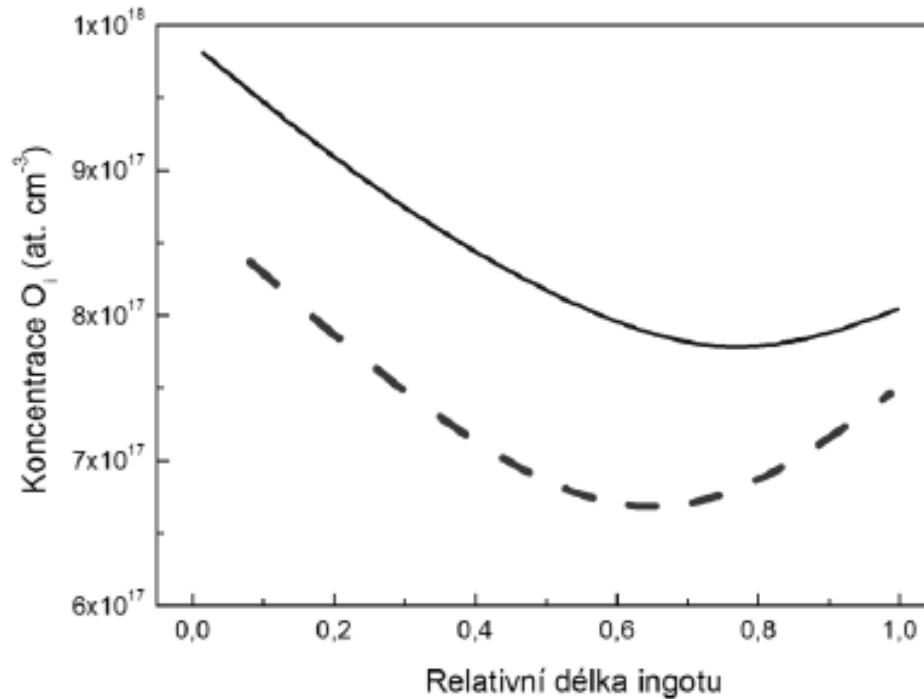
# Axiální profil koncentrace příměsí



Dopant	$k_0$	$c_s^m$ [cm <sup>-3</sup> ]	$g$ [cm s <sup>-1</sup> ]	$\delta_r$ [%]
B	0,8	$6 \times 10^{20}$	$8 \times 10^{-6}$	-25
As	0,3	$1,8 \times 10^{21}$	$8 \times 10^{-3}$	0
P	0,35	$1,3 \times 10^{21}$	$1,6 \times 10^{-4}$	-7
Sb	0,023	$7 \times 10^{19}$	0,13	+15



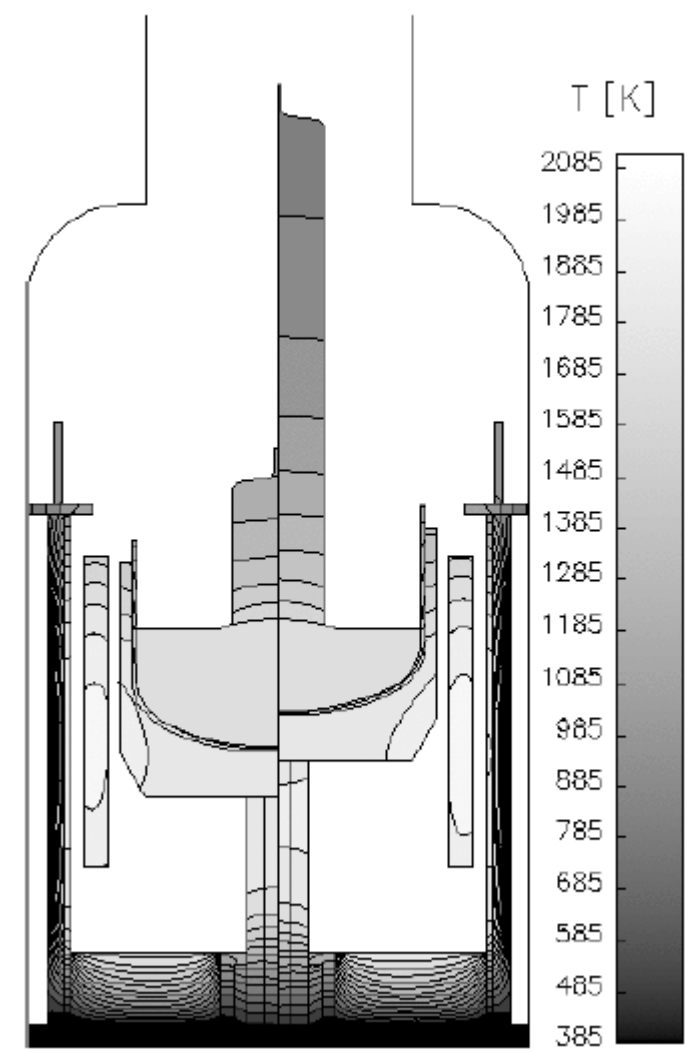
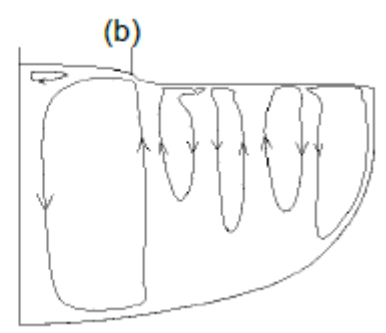
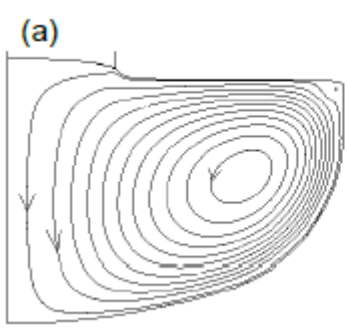
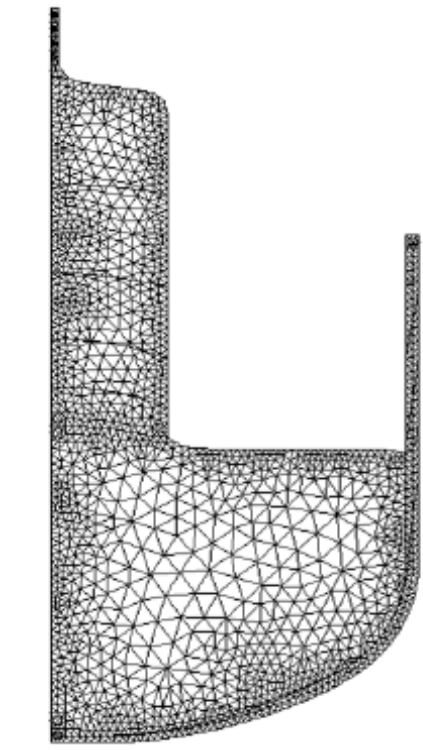
# Axiální profil koncentrace kyslíku



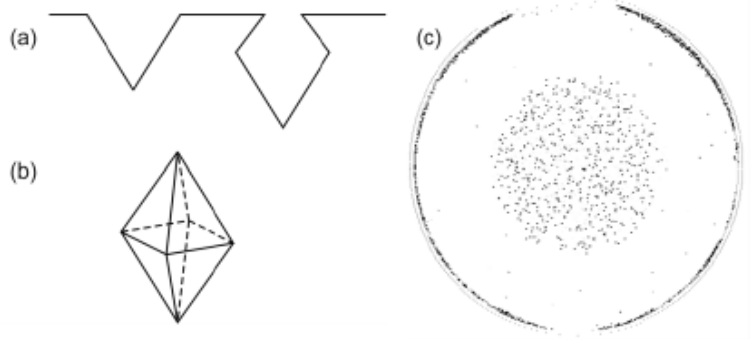
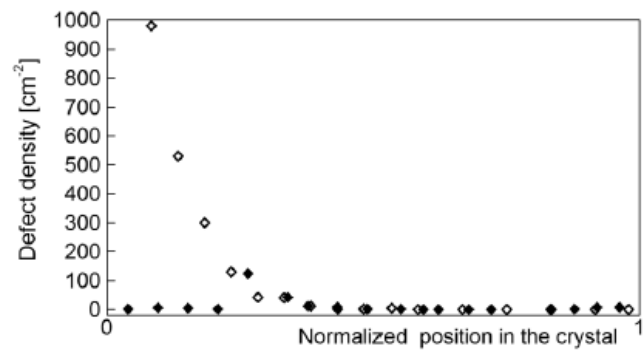
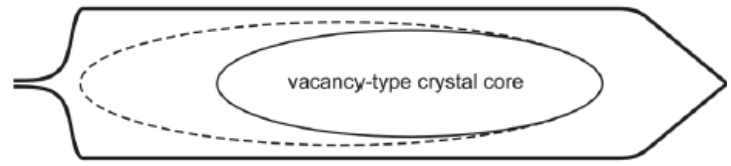
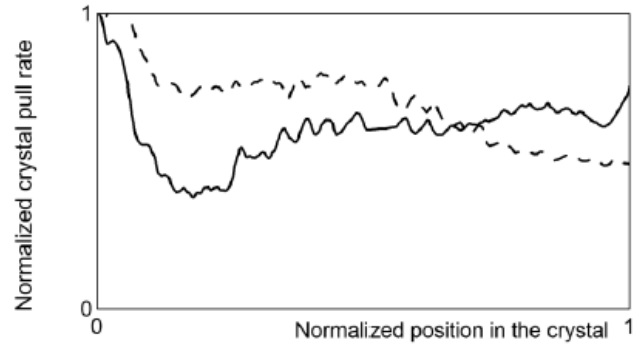
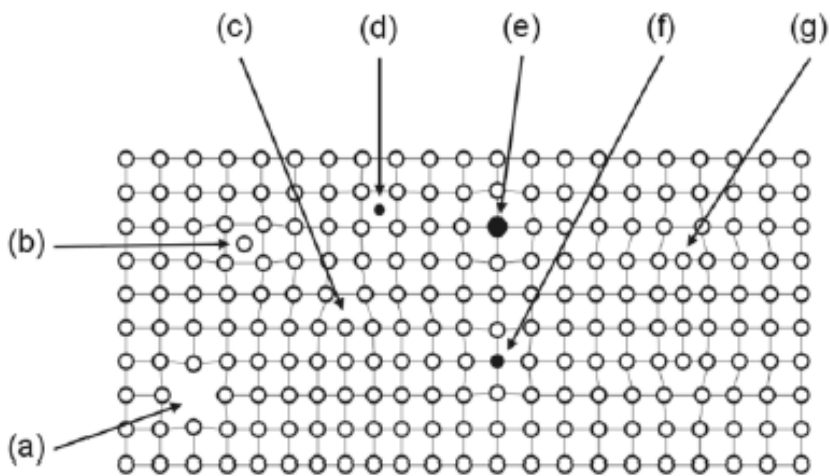
$$[O_2]_{Si} = A_i v C_m = A_c D (C_c - C_m) / (\delta)_c - A_m D C_m / (\delta)_s,$$

kde  $A_i$  je plocha příčného řezu ingotem,  $v$  je rychlost tažení,  $C_m$  je koncentrace kyslíku v tavenině,  $A_c$  je plocha styku kelímek/tavenina,  $D$  je difuzní koeficient kyslíku,  $C_c$  je koncentrace kyslíku ve stěně kelímku,  $(\delta)_c$  a  $(\delta)_s$  jsou tloušťky difuzních vrstev na rozhraní kelímek/tavenina a tavenina/volný povrch,  $A_m$  je plocha volného povrchu taveniny. Z uvedeného vztahu vyplývá především význam rychlosti tažení a poměrů na rozhraní kelímek/tavenina (úzce souvisí s prouděním taveniny v kelímku).

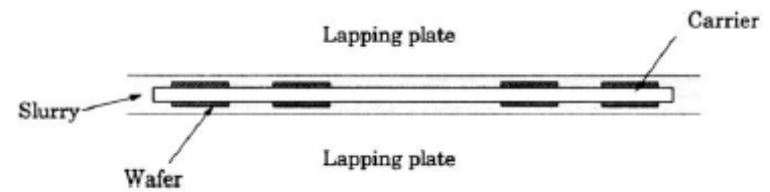
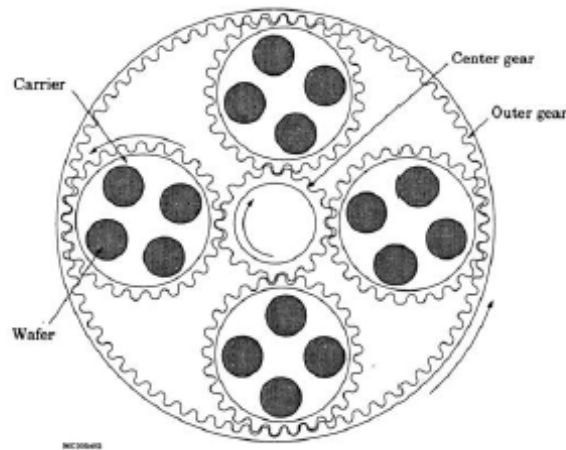
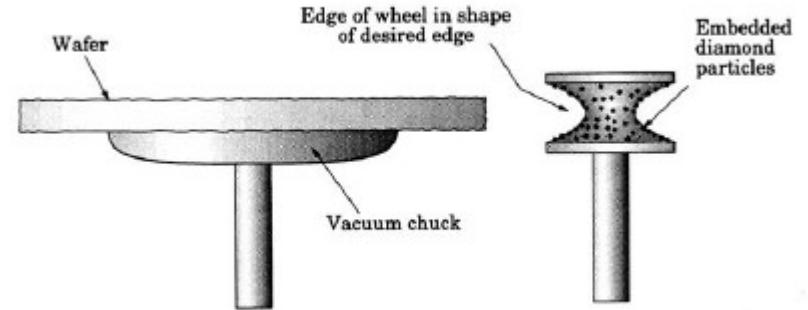
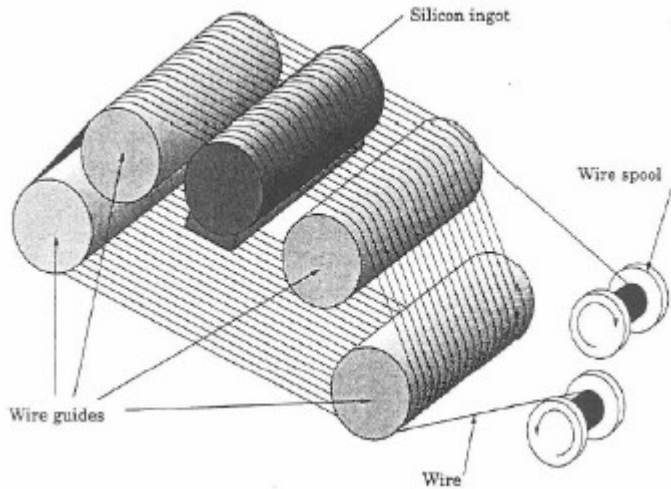
# Simulace metodou konečných prvků



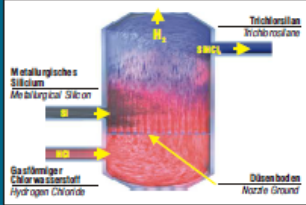
# Mikrodefekty



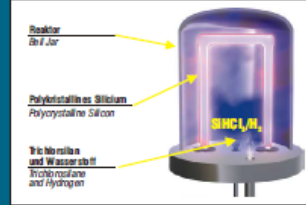
# Výroba křemíkových desek - řezání, zaoblování a lapování



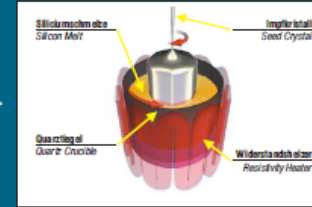
## WIRBELSCHICHTREAKTOR FLUIDIZED BED REACTOR



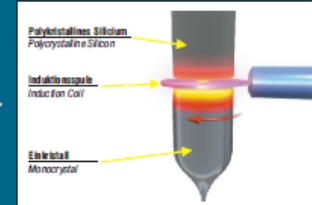
## ABSCHIEDUNG VON POLYKRISTALLINEM REINSTSILICIUM CHEMICAL VAPOR DEPOSITION OF POLYCRYSTALLINE SILICON



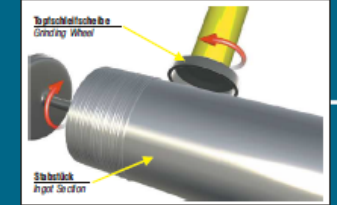
## TIEGELZIEHEN CZOCZRALSKI PULLING



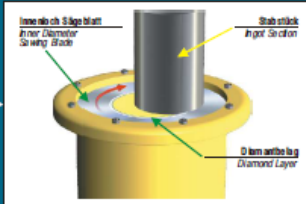
## ZONENZIEHEN FLOAT ZONE PULLING



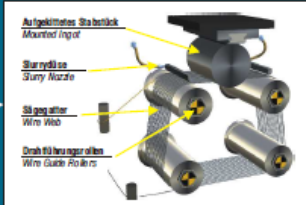
## RUNDSCHLEIFEN INGOT GRINDING



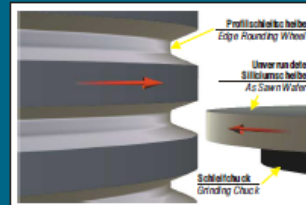
## INNENLOCHSÄGEN INNER DIAMETER SLICING



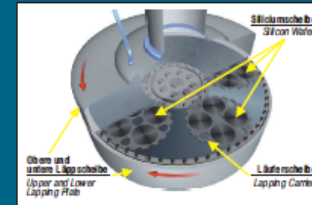
## DRAHTSÄGETECHNIK MULTI WIRE SLICING



## KANTENVERRUNDEN EDGE ROUNDING



## LÄPPEN LAPPING

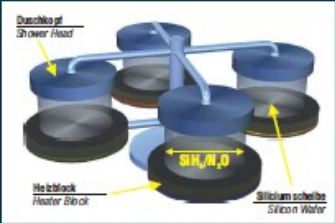


# Flow 2/2

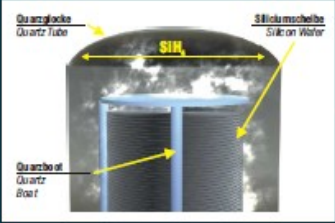
## REINIGEN UND ÄTZEN CLEANING AND ETCHING



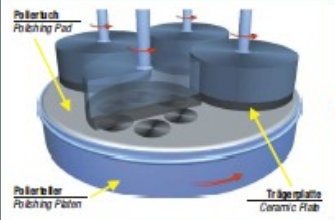
## OXID-BESCHICHTUNG OXIDE DEPOSITION



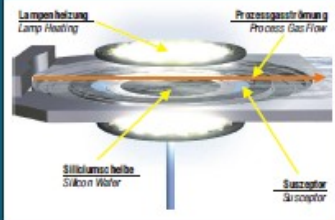
## POLY-BESCHICHTUNG POLY DEPOSITION



## POLIEREN POLISHING



## EPITAXIE EPITAXY

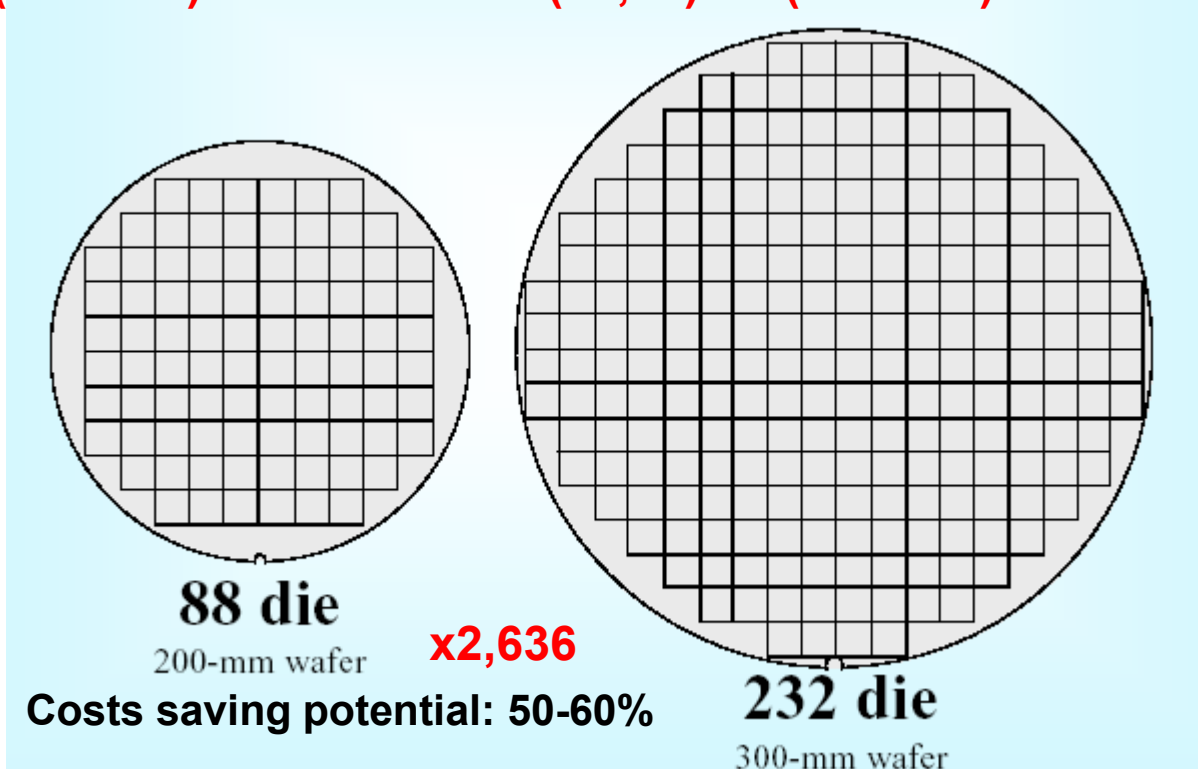


© 2004 Siltronic [www.siltronic.com](http://www.siltronic.com)



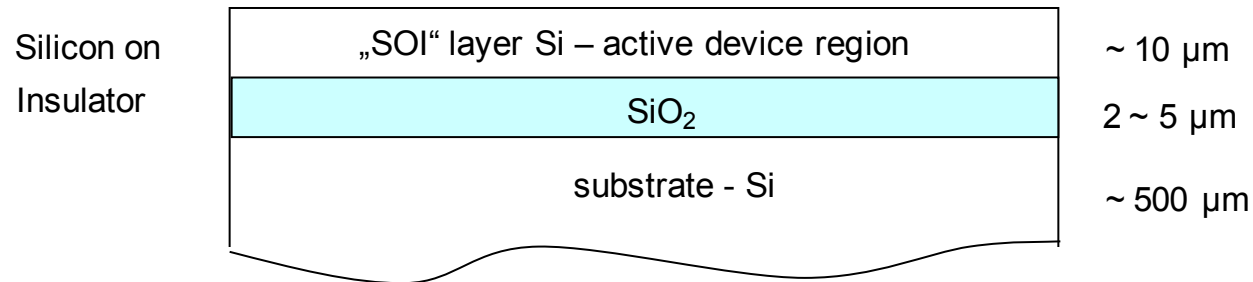
# Důvod zvětšování průměru desek

$$S (200 \text{ mm}) = 31\,400 \text{ mm}^2 \quad (\times 2,25) \quad S (300 \text{ mm}) = 70\,650 \text{ mm}^2$$



# Silicon-On-Insulator

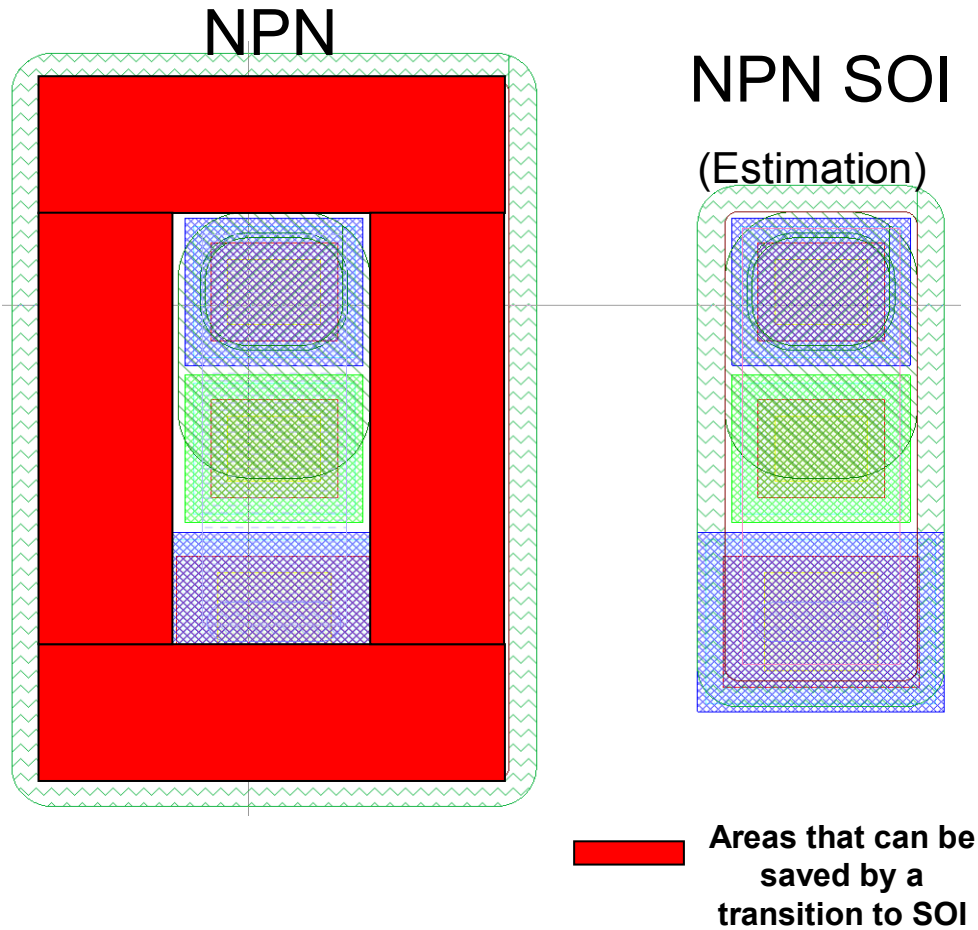
- SOI
  - sSOI
  - SiGeOI
  - GeOI
  - Thick Film SOI
  - Thin Film SOI
  - UTSOI
- Silicon on Insulator
- Strained Silicon on Insulator
- SiGe (silicon germanium) on Insulator
- Germanium on Insulator
- SOI with device layer thickness  $\geq 2\mu\text{m}$
- SOI with device layer thickness  $\leq 2\mu\text{m}$
- Ultra Thin SOI – SOI with device layer thickness  $\leq 50\text{nm}$



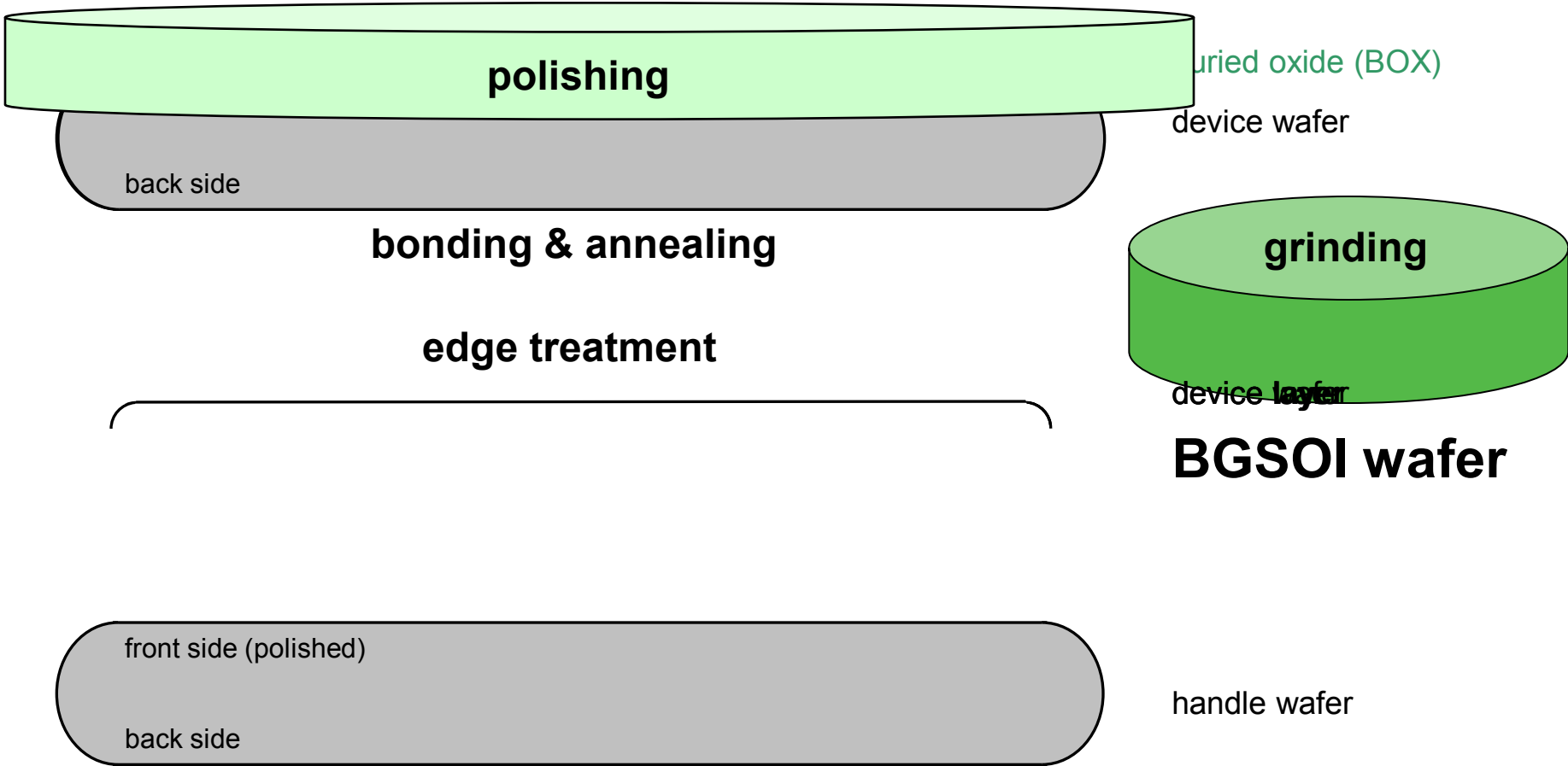


# SOI - příklad „shrink“ součástky

## NPN Transistor – Classical Approach vs. SOI

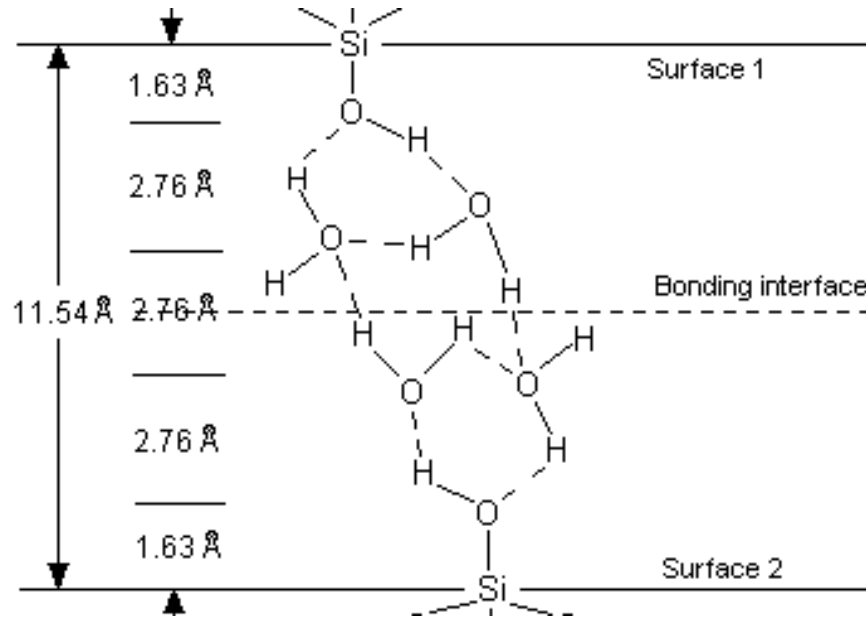


# BGSOI

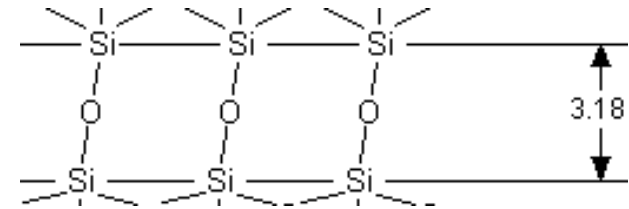


# Bonding leštěných povrchů Si

## Room Temperature Bonding



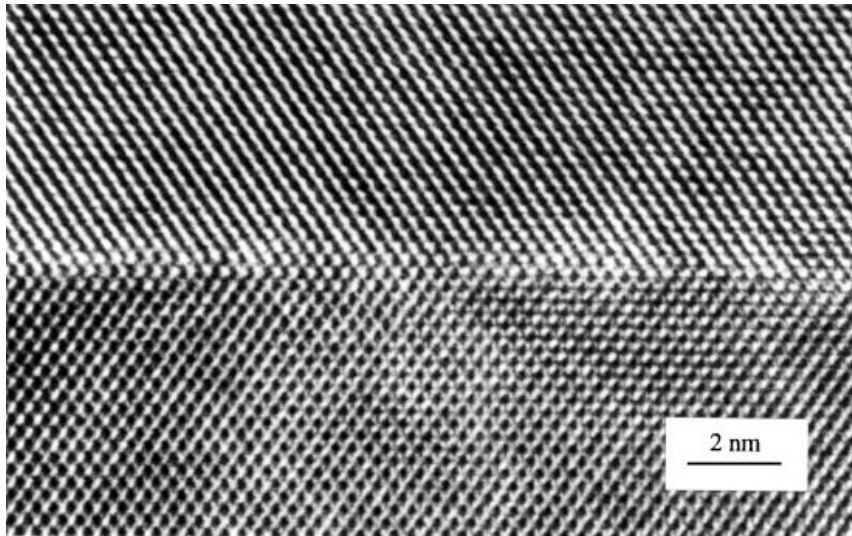
800 °C Annealing



Chemical interface structures of bonded hydrophilic silicon wafers at different temperatures.

Q.-Y. Yong, *Principles of wafer bonding*, in *Silicon Wafer Bonding Technology for VLSI and MEMS Application*, edited by S. S. Iyer and A. J. Auberton-Hervé, INSPEC, The Institution of Electrical Engineers, 2002.

# TEM bondovaného rozhrani



Cross-sectional HRTEM of the interface of Si/Si bonded at room temperature in UHV w/o any further heat treatment.



Cross-sectional TEM image of bonded interface between Si and thermal SiO<sub>2</sub>.

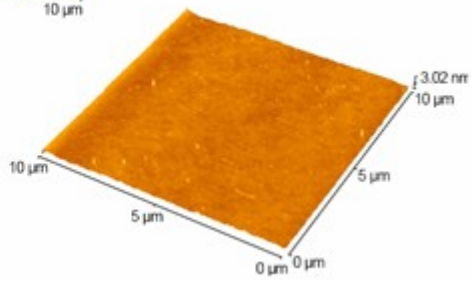
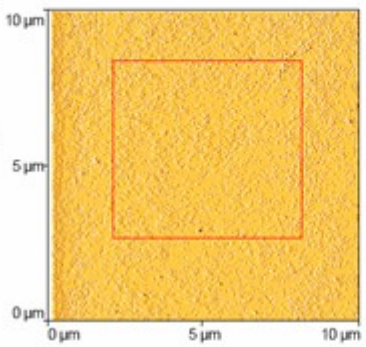
# AFM leštěných povrchů

RMS (1x1μm <sup>2</sup> )	Bonding quality
< 0.15 nm	Excellent
(0.15 – 2) nm	Good to mixed
(2 – 5) nm	Poor
> 5 nm	Impossible

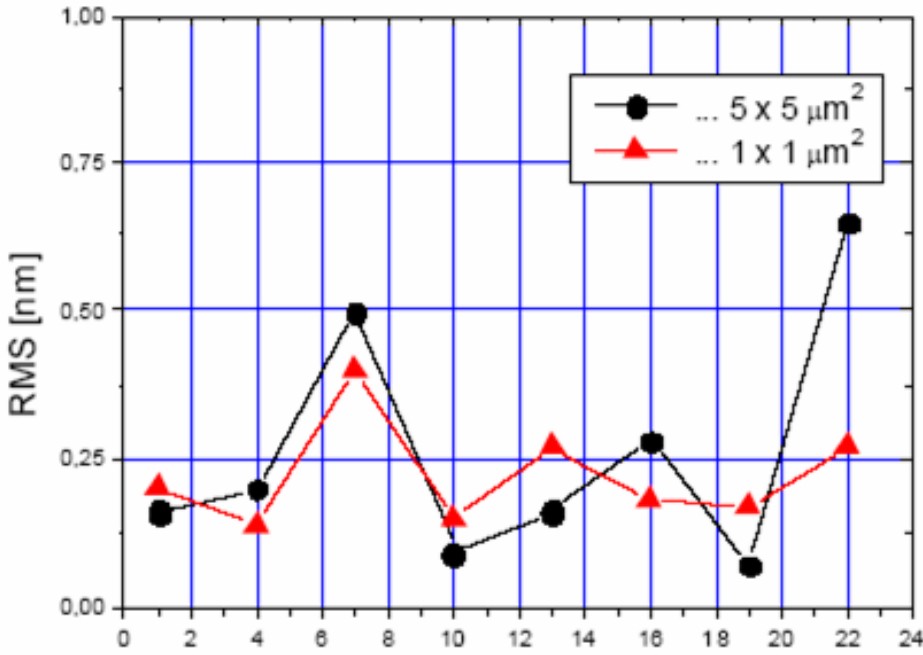
Whole Image:  
 Area Ra: 0.0689 nm  
 Area RMS: 0.1434 nm  
 Avg. Height: 1.1604 nm  
 Max. Range: 3.0218 nm

Partial Image:  
 Area Ra: 0.0604 nm  
 Area RMS: 0.1062 nm  
 Avg. Height: 1.1604 nm  
 Height. Max: 1.7080 nm

Include Area  
 Exclude Area



Ra 0.10 nm  
 RMS 0.14 nm



- similar RMS for 1x1 μm<sup>2</sup> and for 5x5 μm<sup>2</sup>
- CZ2 wafers are suitable for bonding



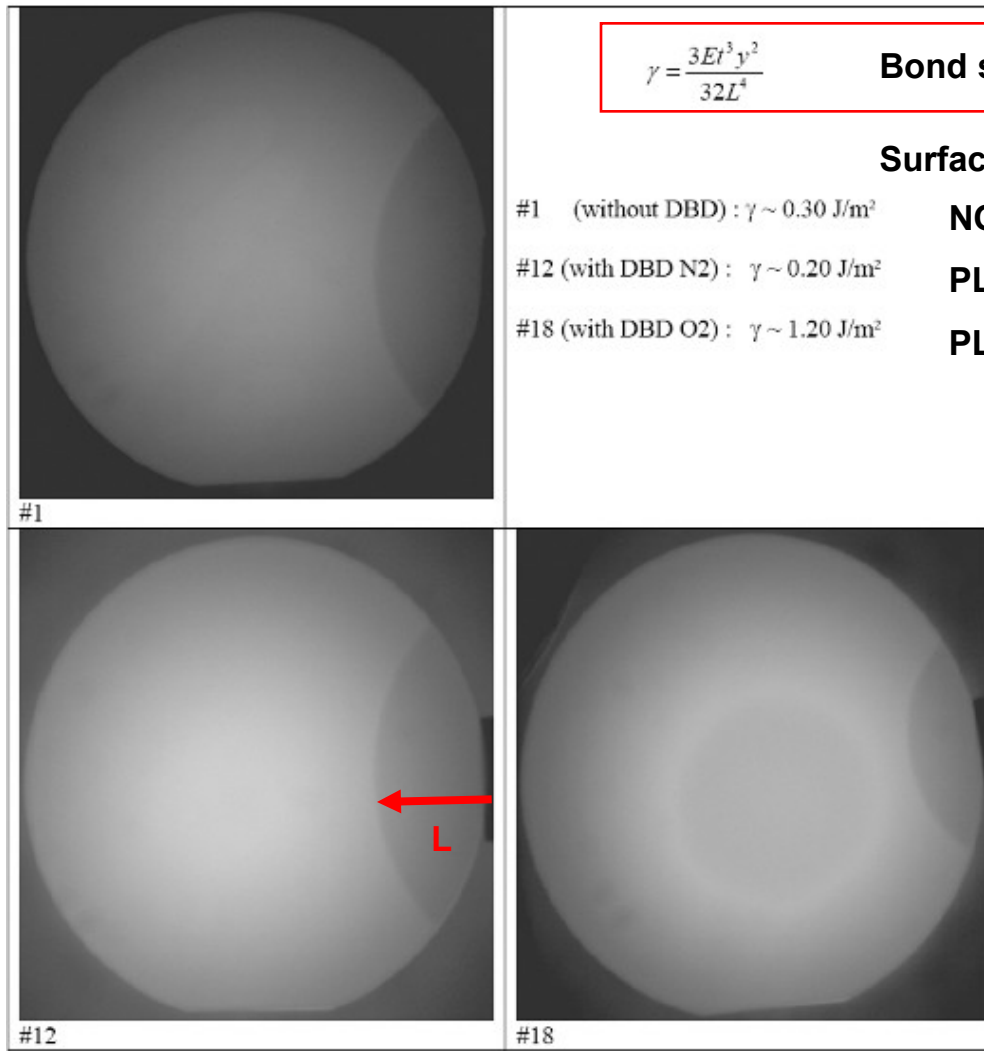
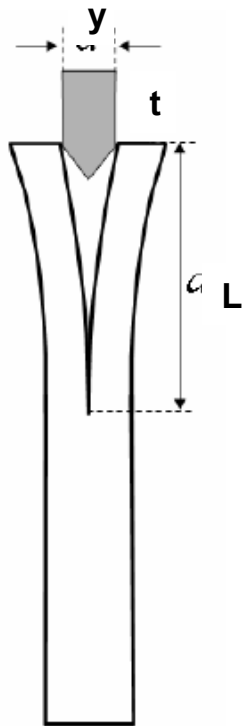
# Analýza síly vazby mezi povrchy desek

E ... Young module

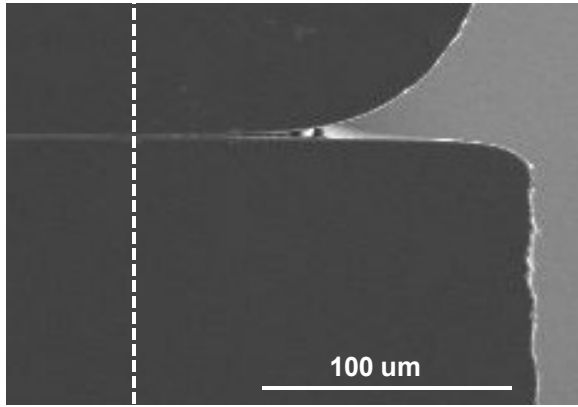
y ... Blade THK (150 μm)

t ... Wafer THK

L ... Length of crack

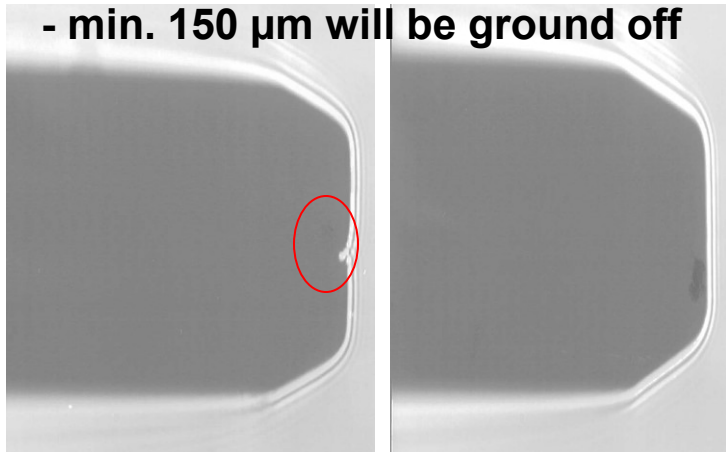


# Úprava okraje SOI desek

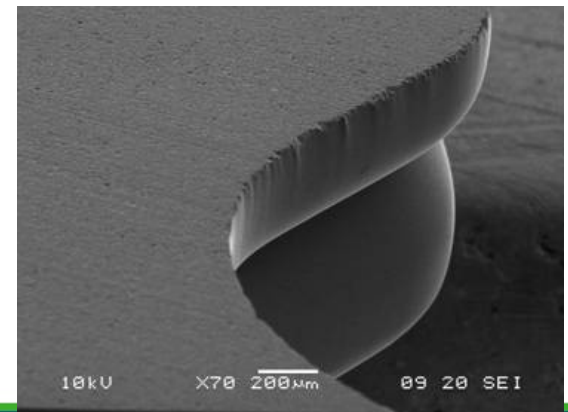


- polished wafer for SOI is made with  $\text{Ø}150.3$  mm,
- asymmetric edge profile for maximizing of bonding area,
- post bond annealing in wet atmosphere (for oxidation of bonded pair edge),
- SOI edge grinding - removal of  $300 \mu\text{m}$  from wafer  $\text{Ø}$ ,
- Profiling of device layer edge (to prevent peeling).

- min.  $150 \mu\text{m}$  will be ground off



- Details of notch confirm alignment accuracy of  $\sim 10 \mu\text{m}$ .
- Alignment is important for bonding of wafers with structures or for both-side technologies.



# Základní metody pro analýzy kvality bondingu (komerční řešení EVG)

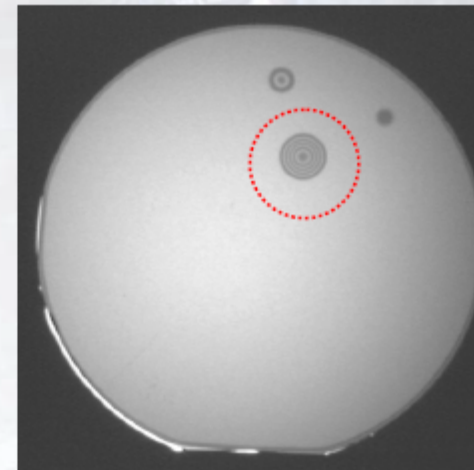
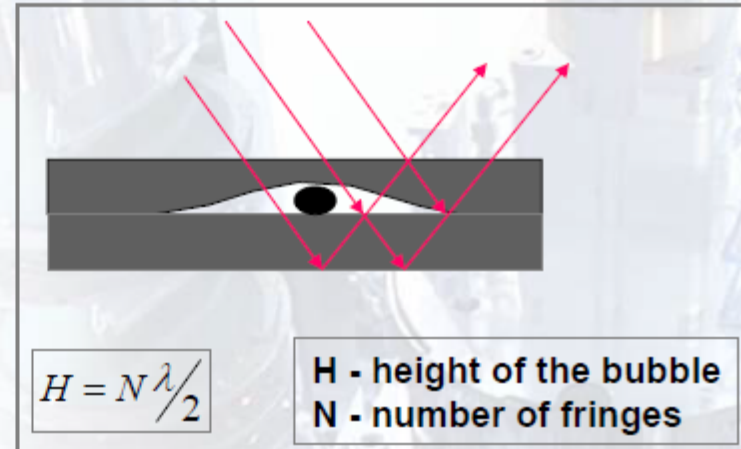


# Infrared Inspection

Material	$E_g$ [eV]	$\lambda$ [ $\mu\text{m}$ ]
Si	1.12	1.10
GaAs	1.43	0.86
InP	1.35	0.91
Ge	0.67	1.84
$\alpha$ -SiC (3C-SiC)	2.2	0.56
$\beta$ -SiC (6H-SiC)	2.93	0.42
GaN	3.4	0.36
AlN	6.2	0.20
SiO <sub>2</sub> (Quartz)	8	0.15
ZnS	3.6	0.34
C (Diamond)	5.48	0.22

Minimum wavelength for which the materials are transparent

$$\lambda = \frac{hc}{E_g}$$



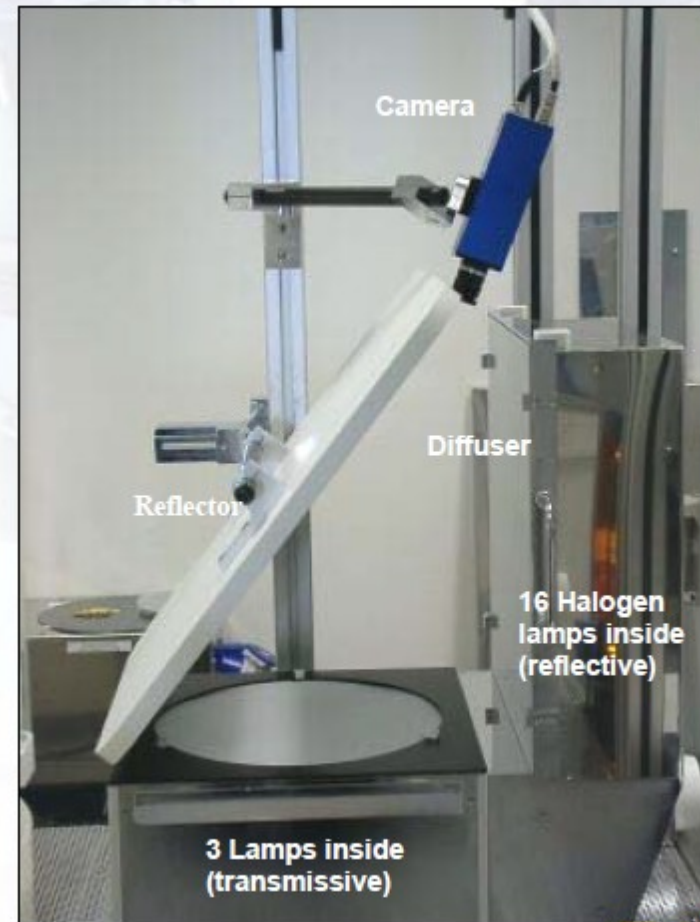
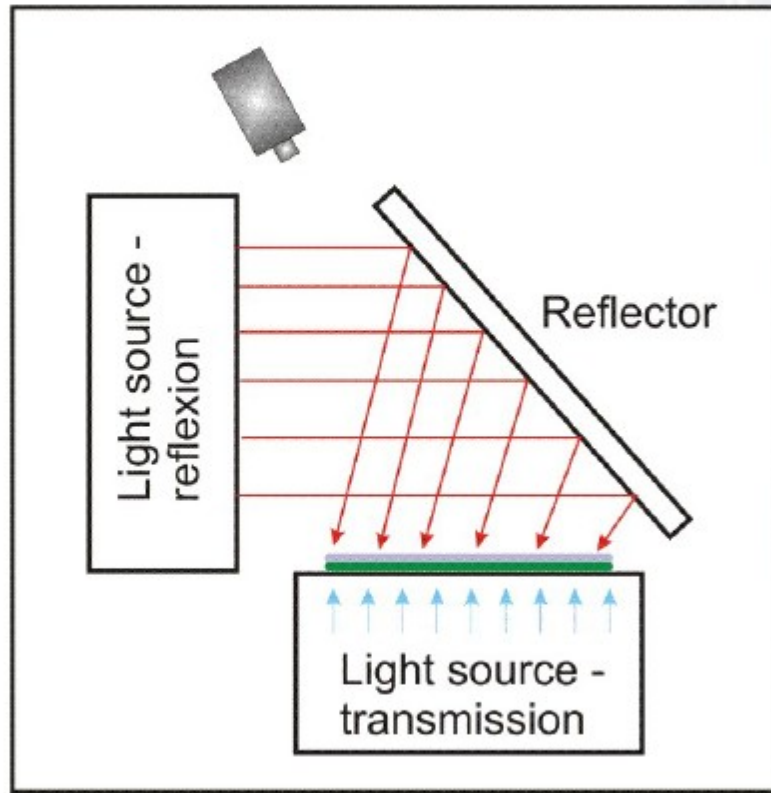
IR transmission image of a bonded wafers pair



EV Group Confidential and Proprietary



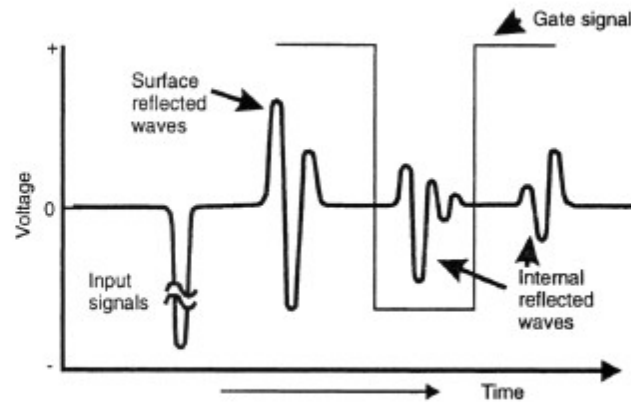
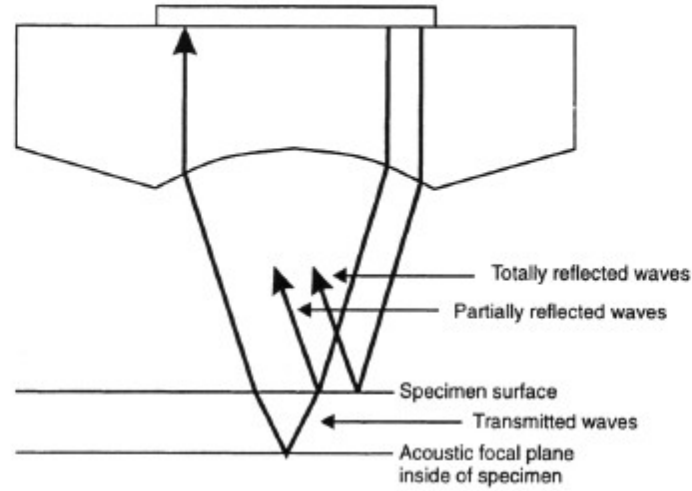
# Transmissive/Reflective IR Inspection stage



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# SAM

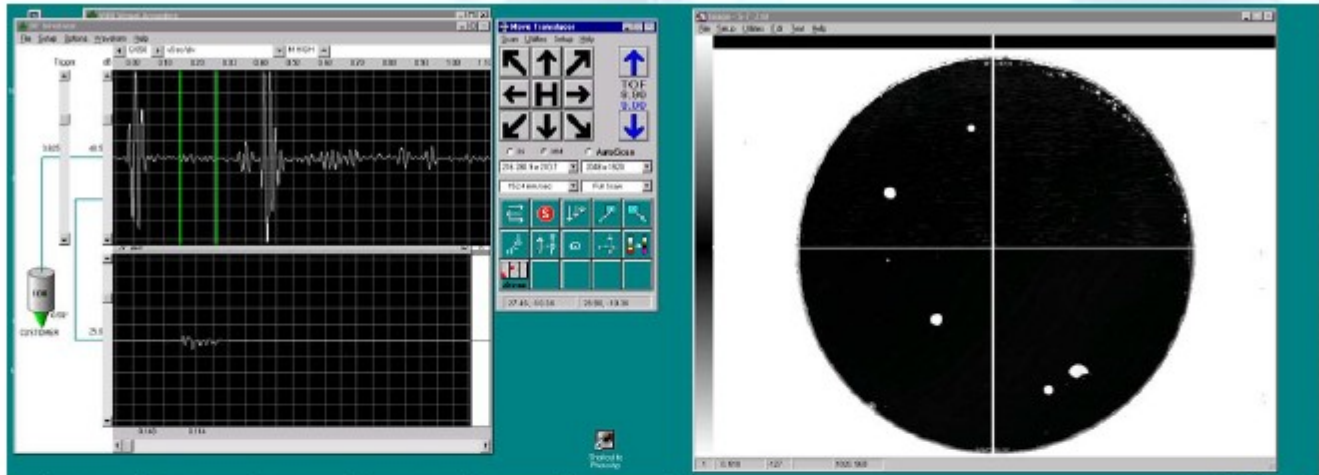


EV Group Confidential and Proprietary

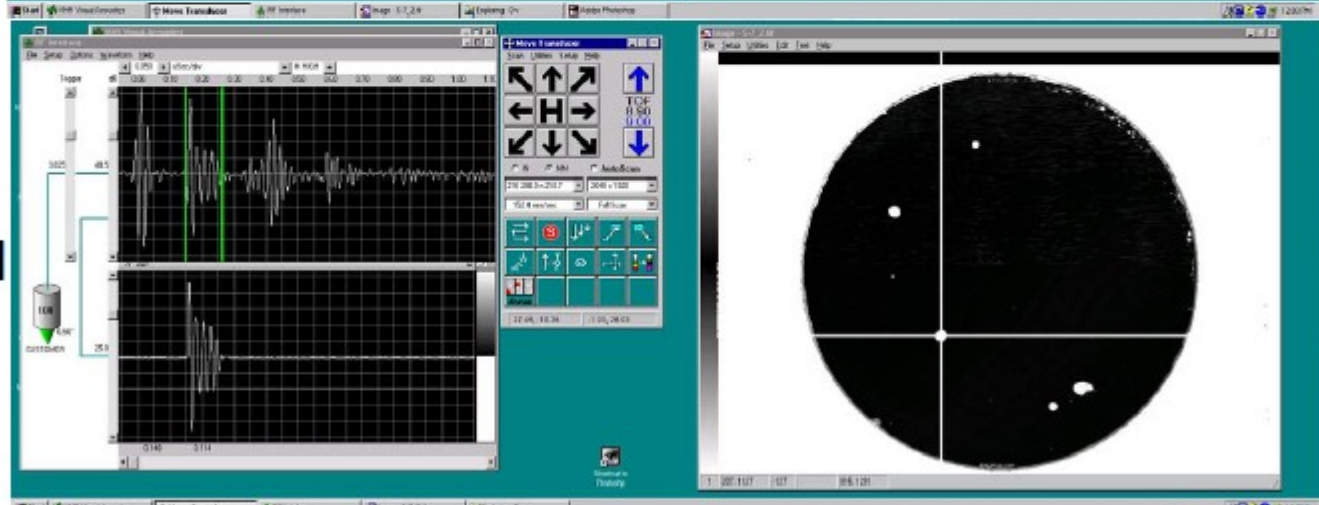


# SAM

Bonded



Unbonded

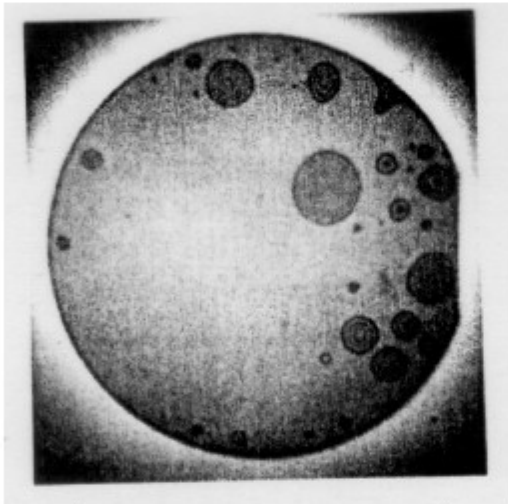


EV Group Confidential and Proprietary



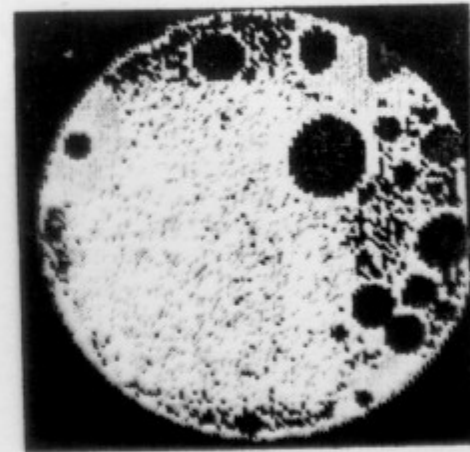
# Comparison Between Different Methods

↔ resolution: 1 mm  
↕ 275 nm @  $\lambda = 1.10 \mu\text{m}$



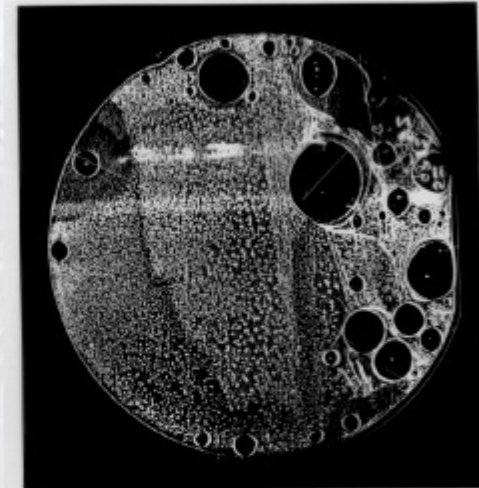
IR transmission

- ↔ resolution: 4  $\mu\text{m}$   
- ↕ resolution: 10 nm



Acoustic imaging

↔ resolution: 2  $\mu\text{m}$



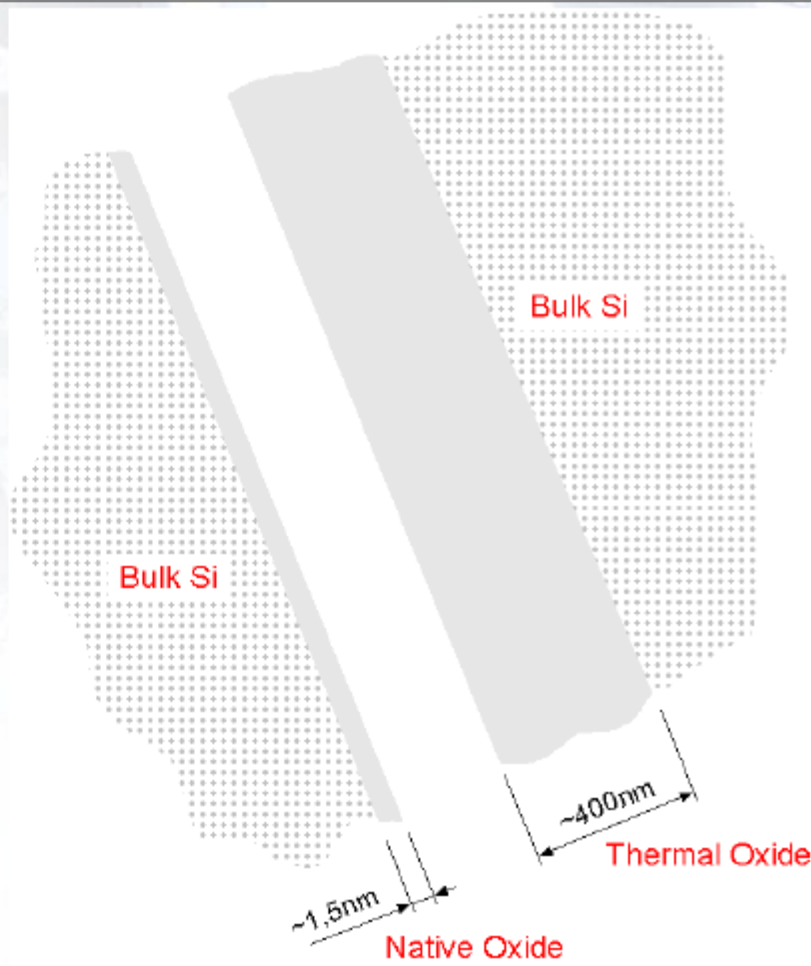
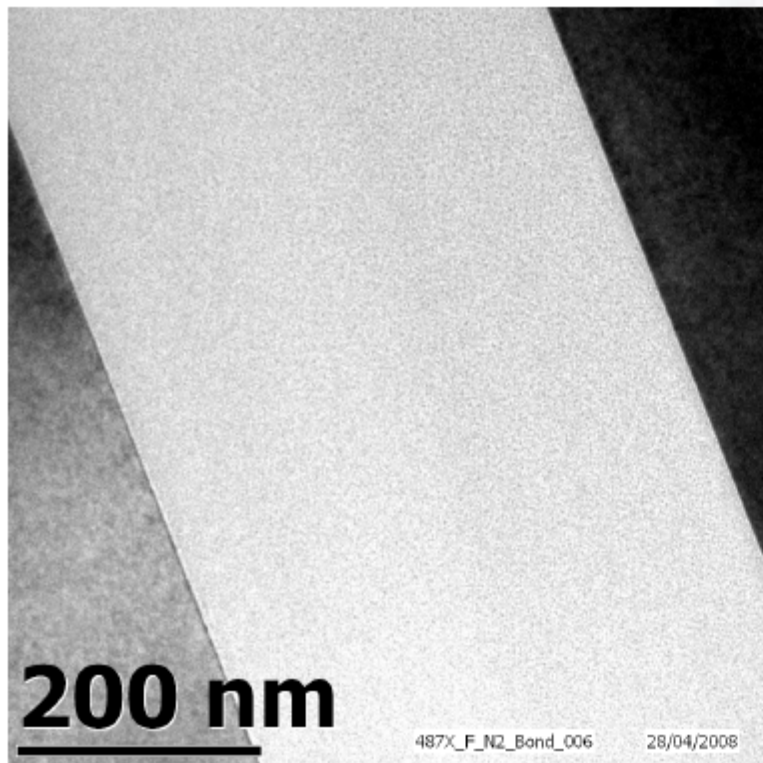
X-ray topography



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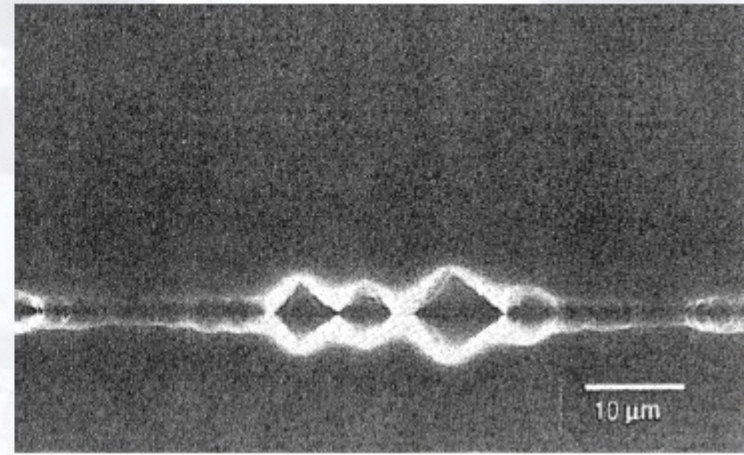
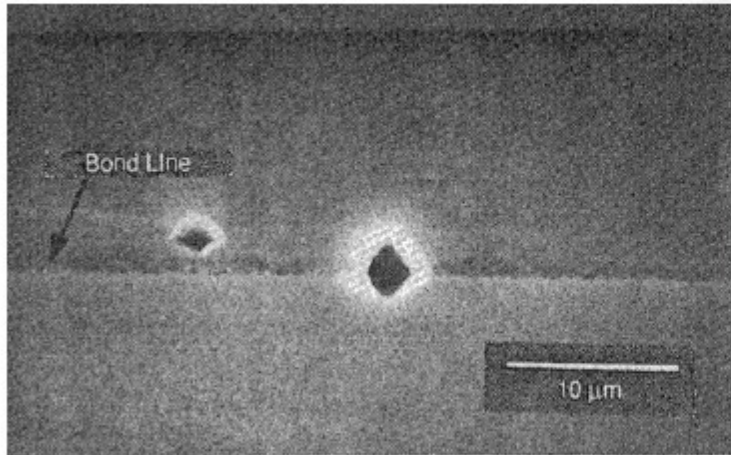
# TEM Analysis



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# Voids Decoration



## Decoration of interface defects by etching of cleaved specimens

### Etching solutions:

- KOH @ 90°C (Si)
- H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (III-V compounds)

### Investigation method:

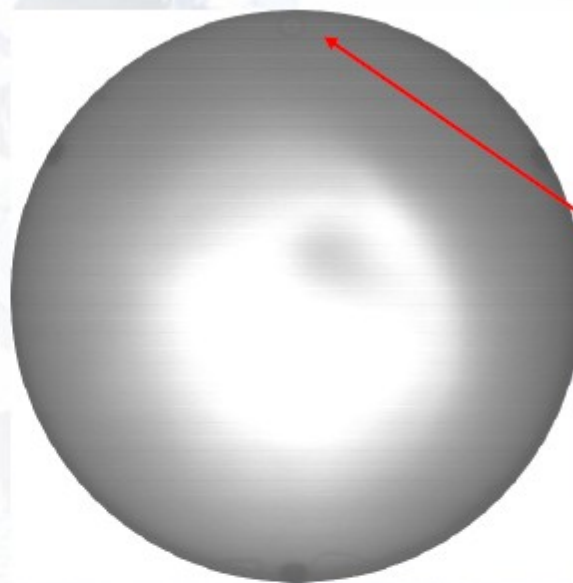
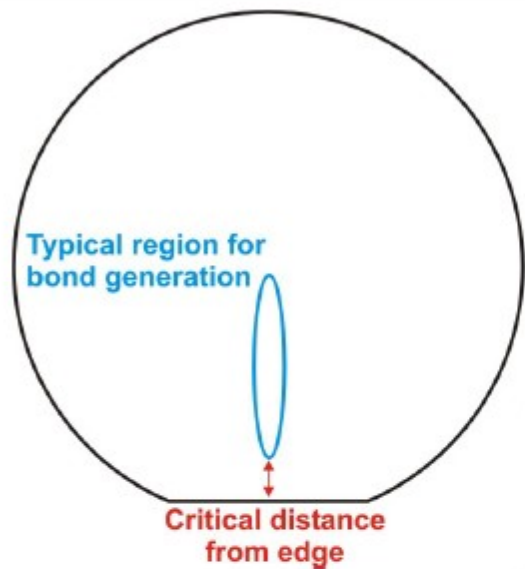
- Optical microscope
- SEM



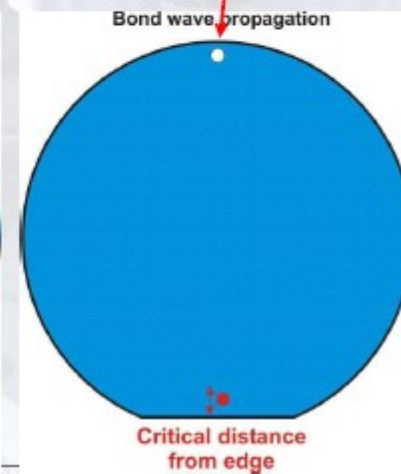
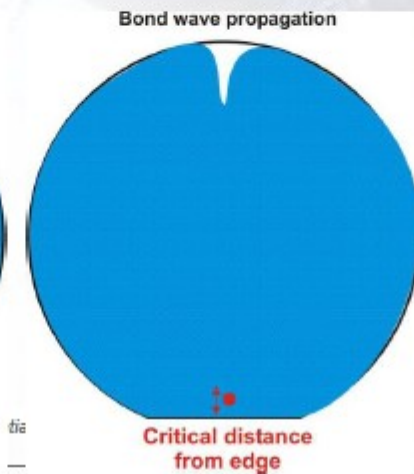
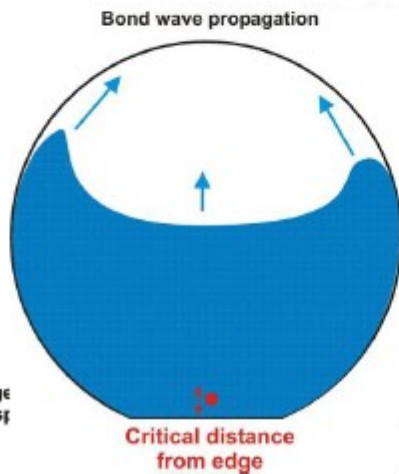
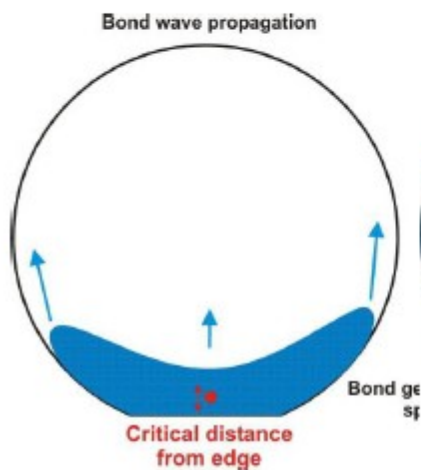
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# Bond Front Generation – „Capture Defects“



„Capture Defect“

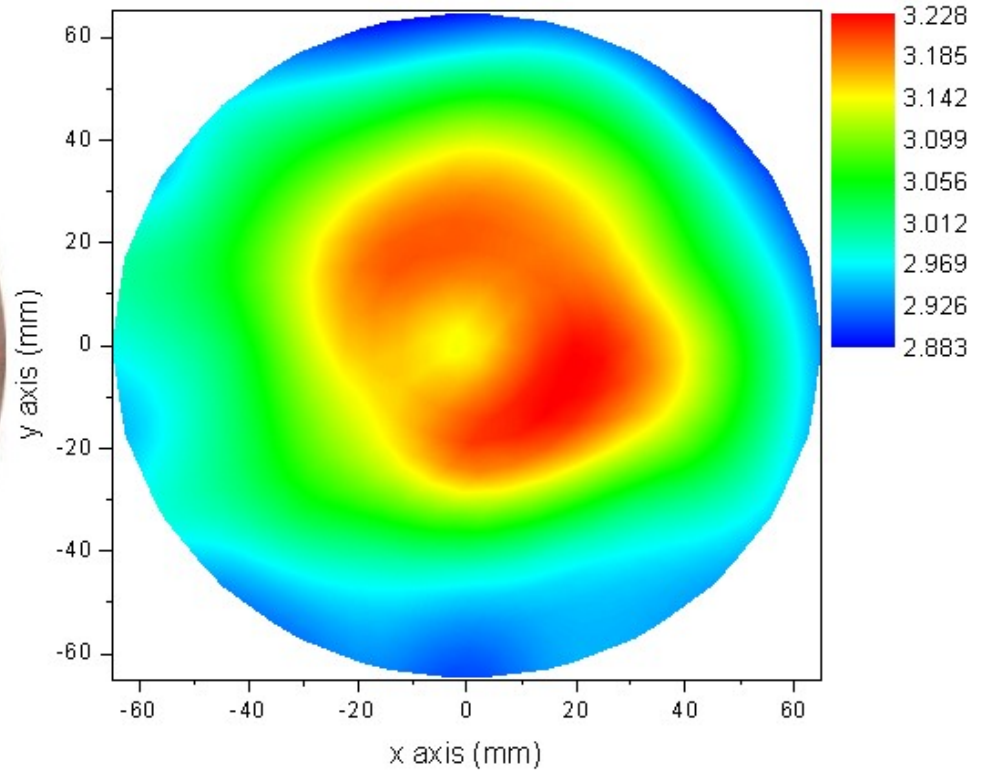




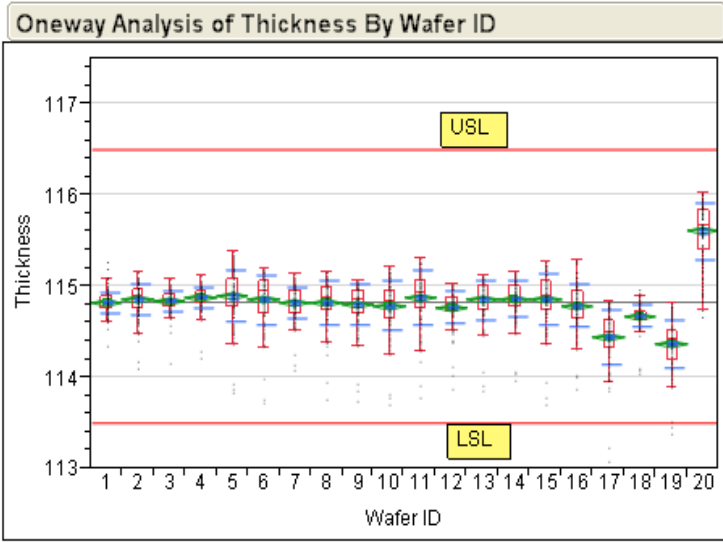
# ONCR/BGSOI

H559 (BGSOI for HFVR, W660S00, LOT MP1106133, #20, JUN 2011)

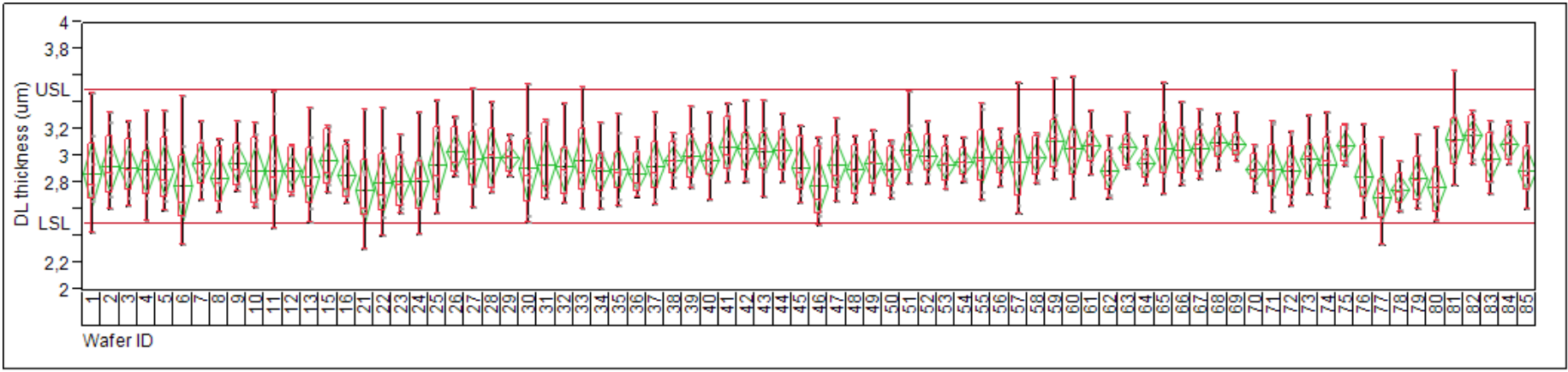
Device layer thickness:  $3.02 \mu\text{m} \pm 0.17 \mu\text{m}$  (target  $3.0 \mu\text{m} \pm 0.5 \mu\text{m}$ )



# BGSOI - manufacturing



- Precise targeting of the grinding and polishing stock removals.
- Examples of two lots with device layer thickness targets of 115,0 and 3,0  $\mu\text{m}$ .
- Usual within-wafer thickness variability of 0,5 – 1,0  $\mu\text{m}$ .
- Usual within-lot thickness variability of 1,0  $\mu\text{m}$ .



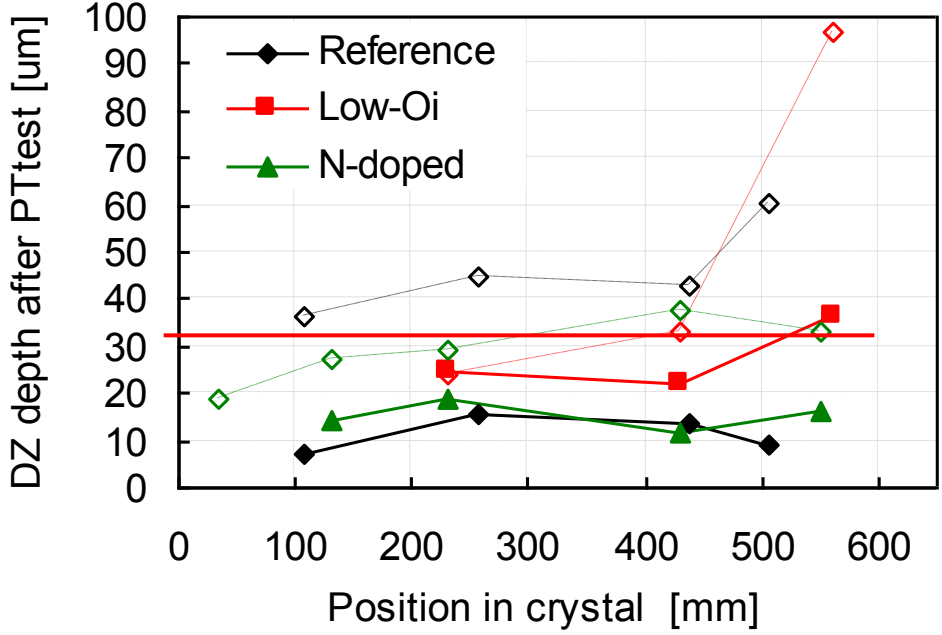
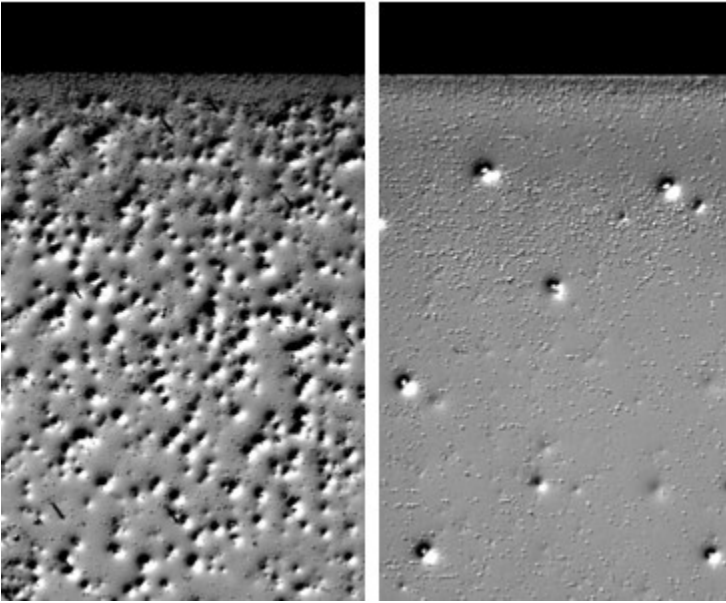
# Defect-free CZ Si - Bulk

## Denudation annealing

- 1200°C / 2hrs, N2 + 0,5% O2
- dissolution of grown-in oxygen precipitates
- oxygen outdiffusion
- denuded zone

polished

DZ annealed



# Defect-free BGSOI Device Layer

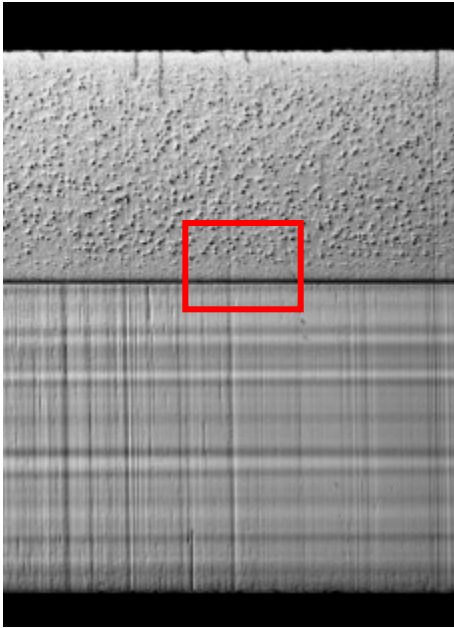
## SOI (HFVR materials)

Si:B, 12 Ohm.cm, 380 um
Si:P, 0.002 Ohm.cm, 525 um

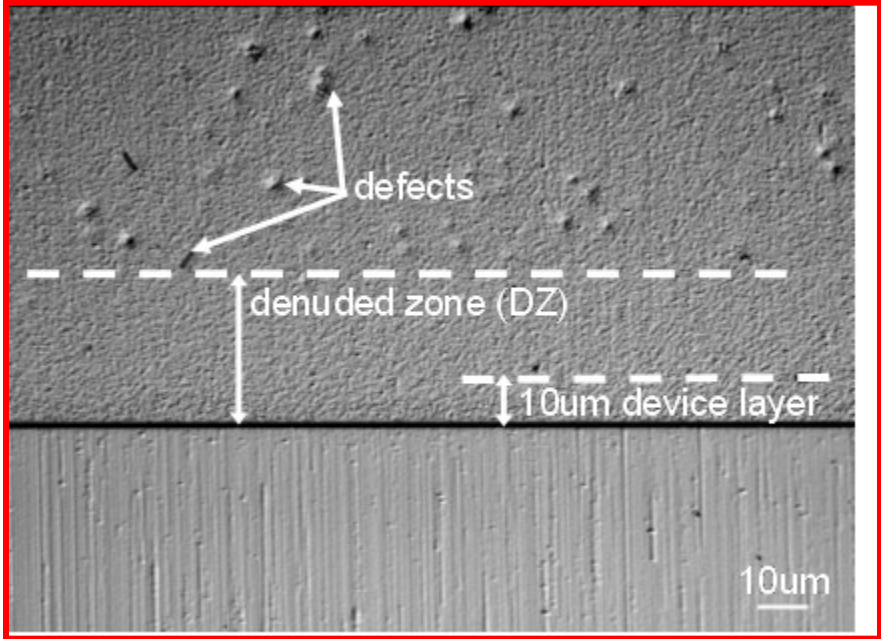
device wafer  
buried oxide  
handle wafer

## Formation of buried oxide on device wafer:

- load & ramp-up
- **DZ annealing** (1200°C/2 hrs, N2+0,5%O2)
- thermal oxidation (1100°C/50 min, wet O2)
- ramp-down & unload



device wafer  
buried oxide  
handle wafer

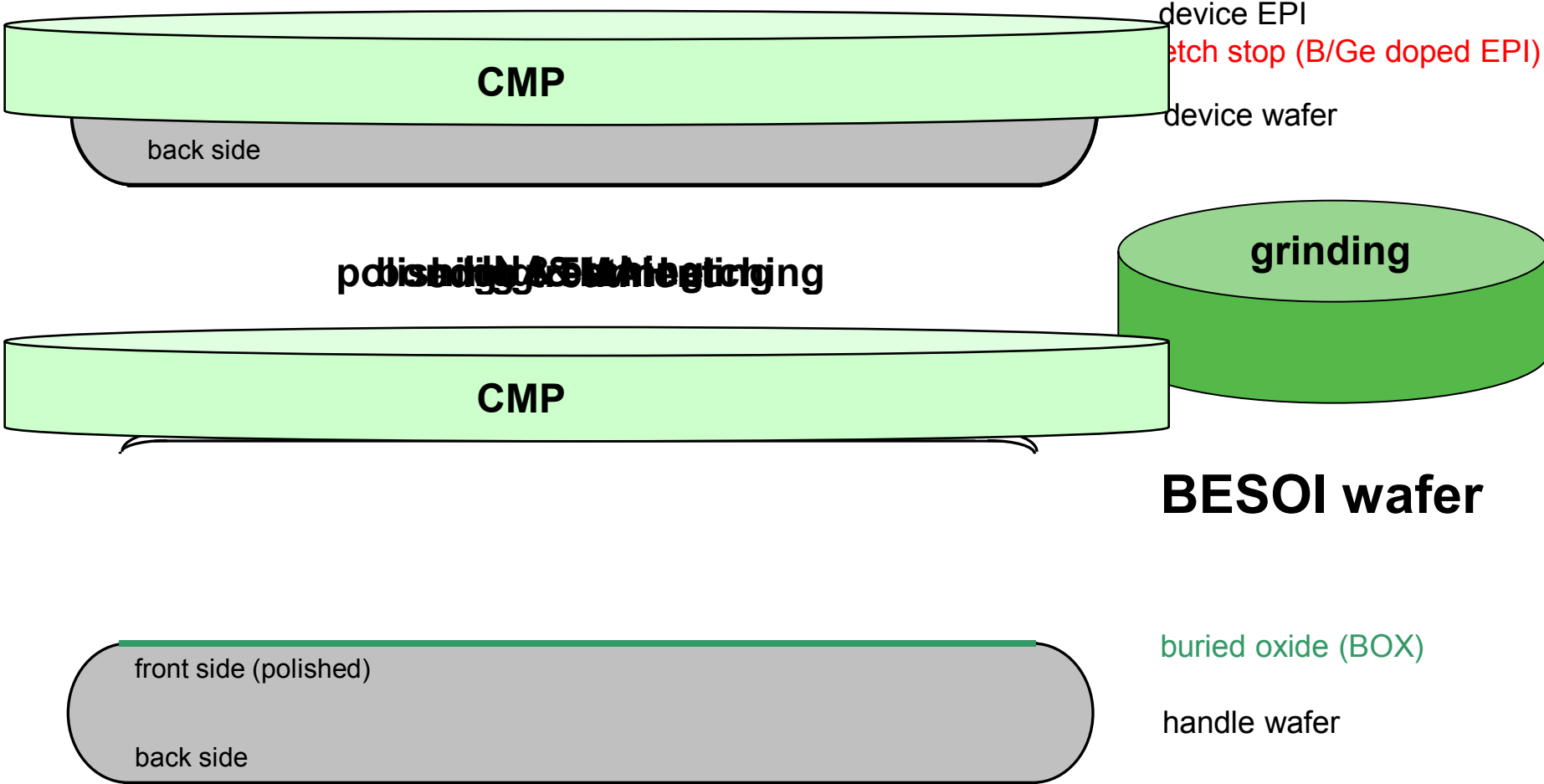


# Comparison of SOI Manufacturing Technologies

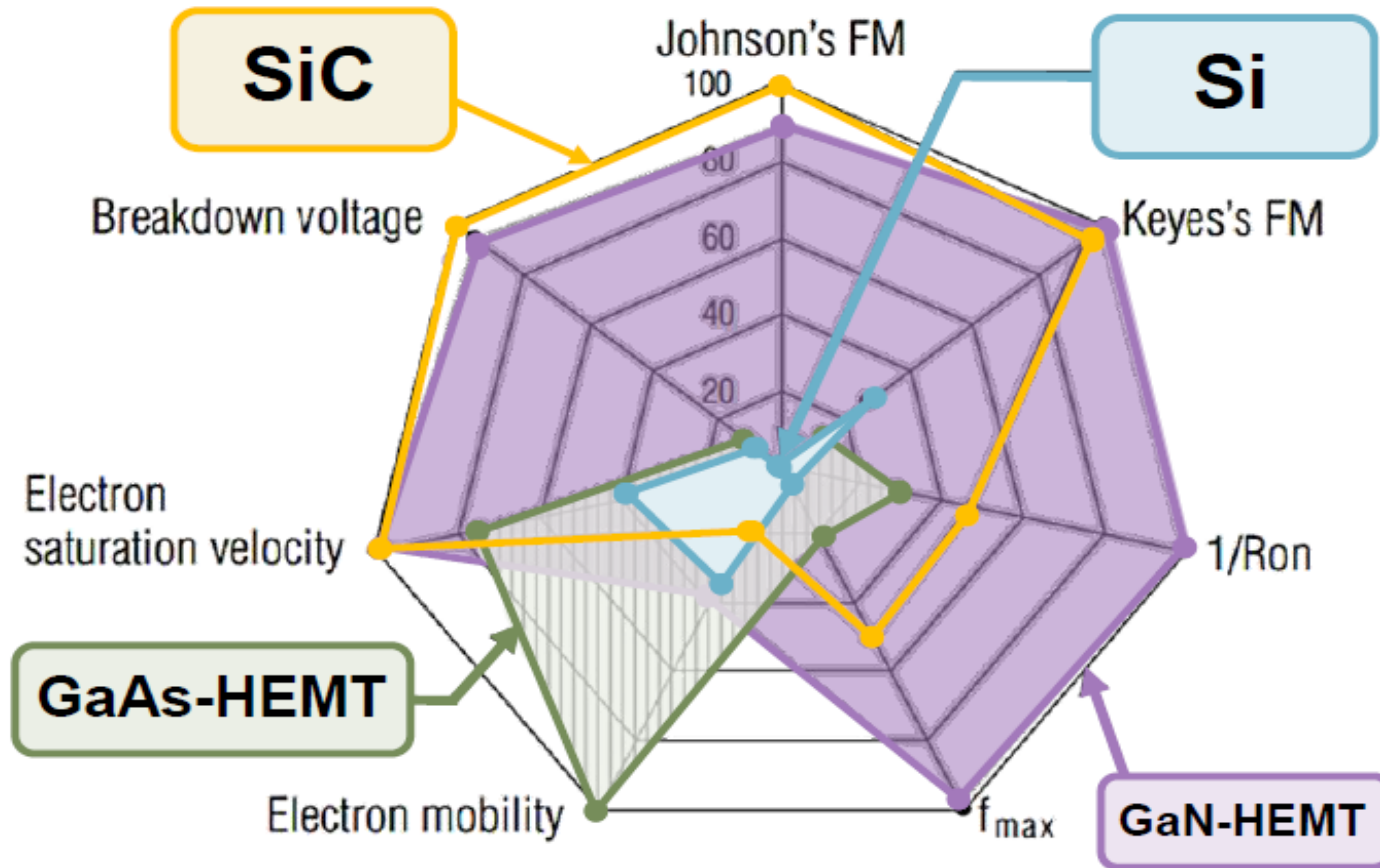
	BGSOI	BESOI	Smart Cut <sup>®</sup>	ELTRAN <sup>®</sup>
Thinning process	mechanical grind and polish	mechanical grind, polish and chemical etch	cleave along plane defined by H implant	cleave along stressed porous Si layer, chemical etch
Factors determining layer uniformity and target	base wafer flatness, mechanical control of grind and polish	epi layer uniformity, chemical etch selectivity and CMP	implant uniformity, CMP	epi layer uniformity, chemical etch selectivity
Reference surface	bottom of handle wafer	top surface of SOI layer	top surface of SOI layer	top surface of SOI layer
Wafer surface finish	CMP	CMP	CMP	hydrogen anneal
Active layer type	bulk of epi	epi	bulk of epi	epi
Uniformity	-	+	+	+
Donor wafer recyclable	-	-	+	+
Thick layers ( $t_{si} > 1.5 \mu$ )	++	+	0 (only with epi deposition)	+
Active layer box interface	thermal oxide	bonded interface	thermal oxide	thermal oxide
Ultrathin layers ( $t_{si} < 0.1 \mu$ )	--	+	0	+
Residual doping	controlled by device wafer	determined by etch-stop out-diffusion	controlled by device wafer of epi	controlled by epi and porous Si process
Strengths	high quality and low cost for thick layers	layer quality, flexibility in active/BOX layer thickness, no implantation	flexibility of active layer type (bulk or epi), relatively simple, high throughput process	layer quality, flexibility in active/BOX layer thickness, no implantation and no CMP
Limitations	not suitable for $t_{si} < 1 \mu$ and demanding uniformity specs	not compatible with high temperature bonding, susceptible to epi defects	possibility of implant damage (?), limitations for ultrathin Si/BOX combinations	high boron concentration in porous Si and BOX layer, susceptible to epi defects
Cost	++	-	+	+

S. S. Iyer, in Silicon wafer bonding technology for VLSI and MEMS applications, (ed. S. S. Iyer, A. J. Auberton-Hervé), INSPEC, London 2002

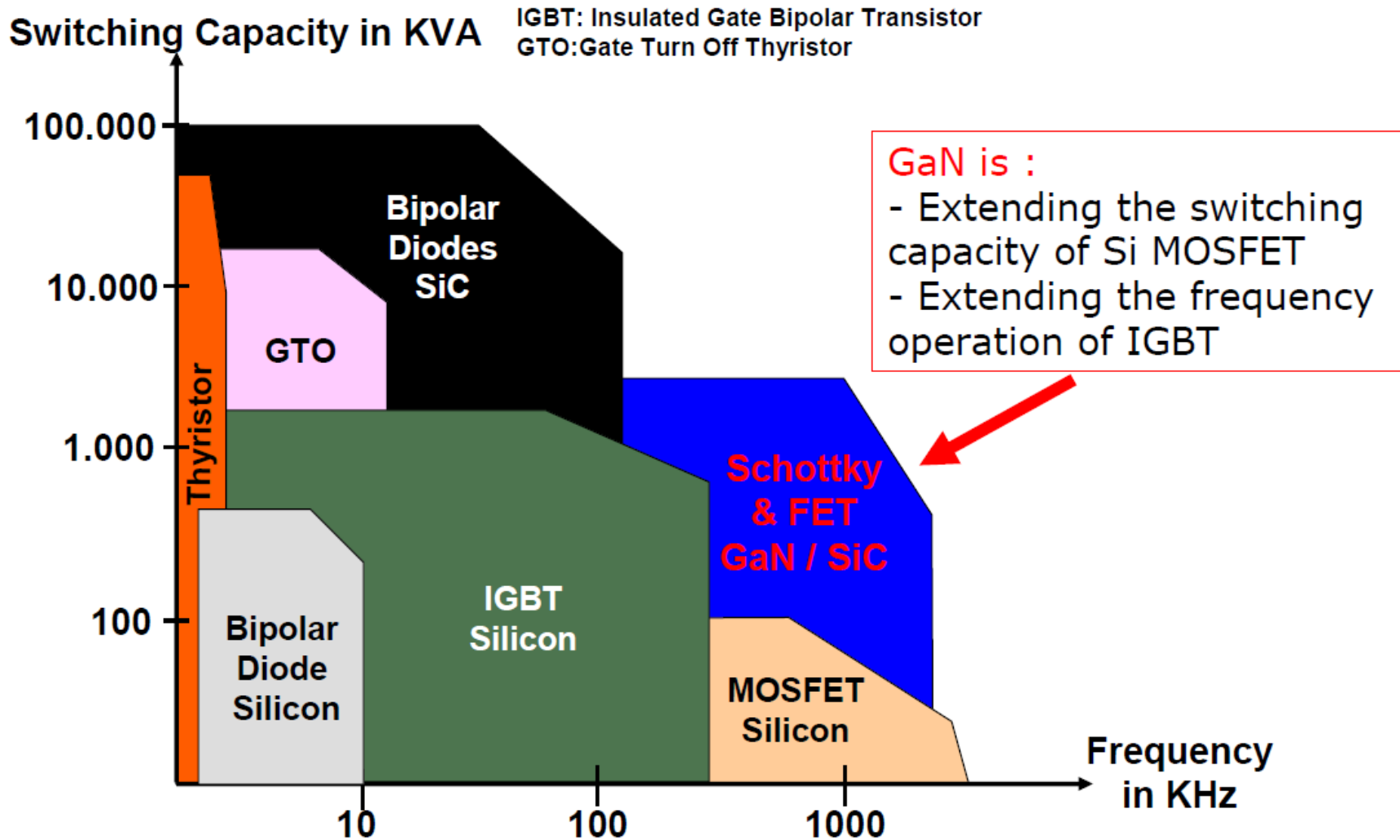
# BESOI



# Perspektivní polovodičové materiály

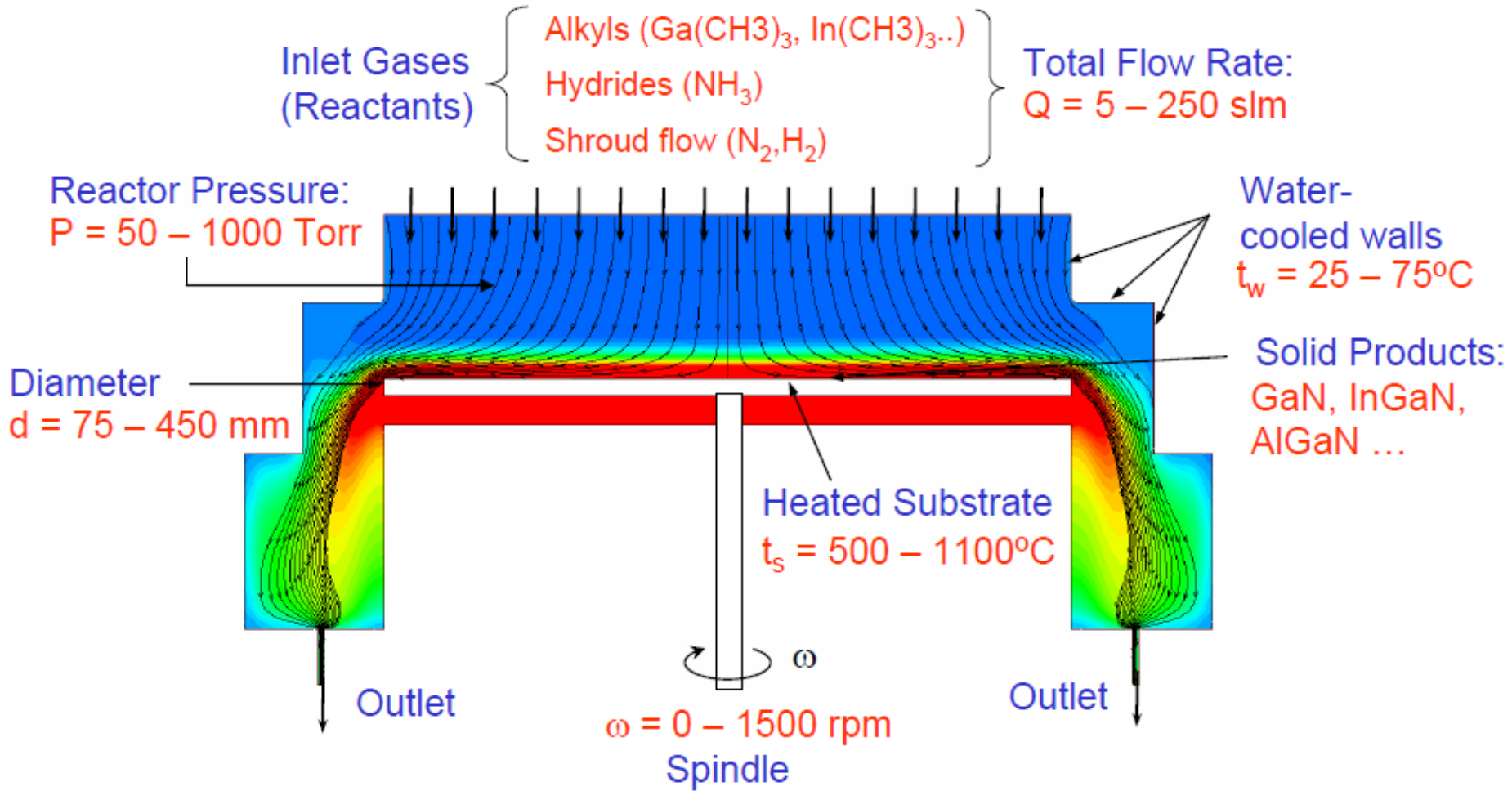


# Výkonová polovodičová řešení



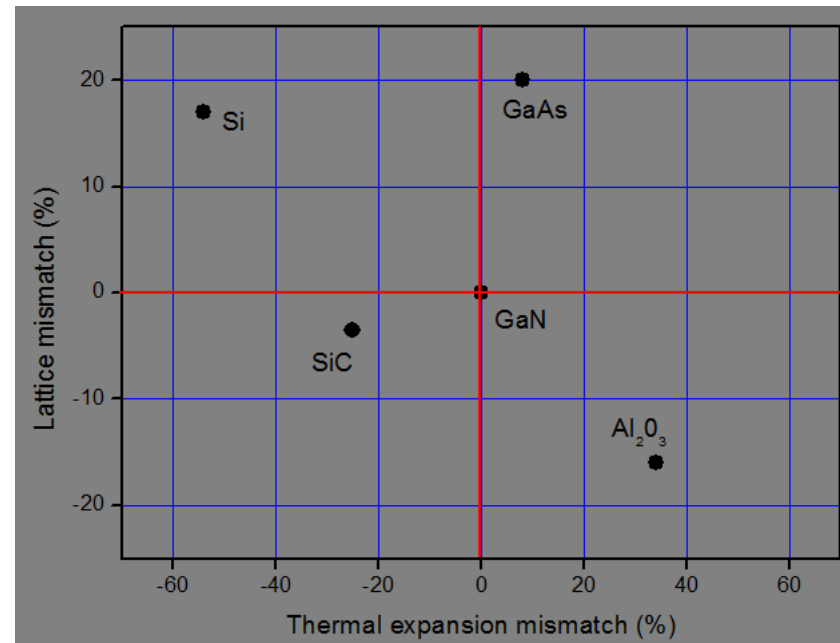


# MOCVD proces pro růst Ga(Al)N/Si

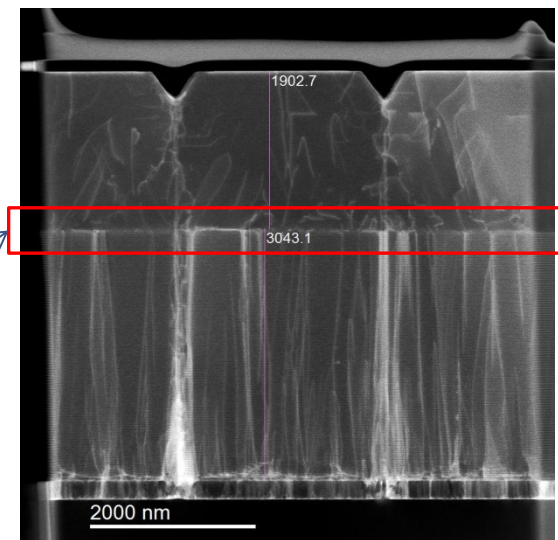
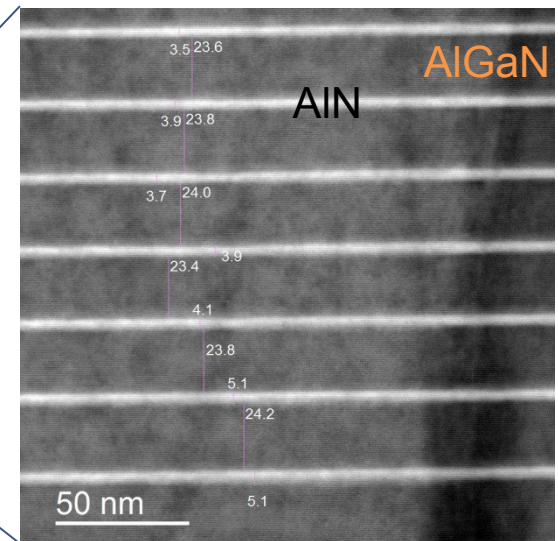
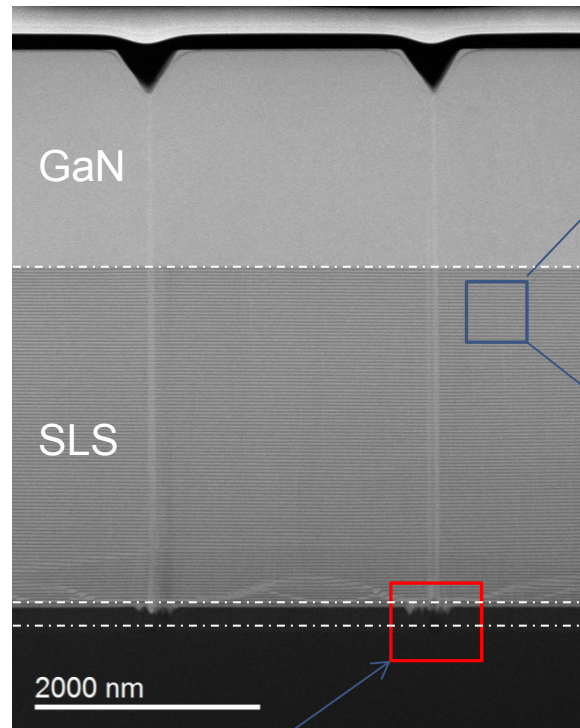
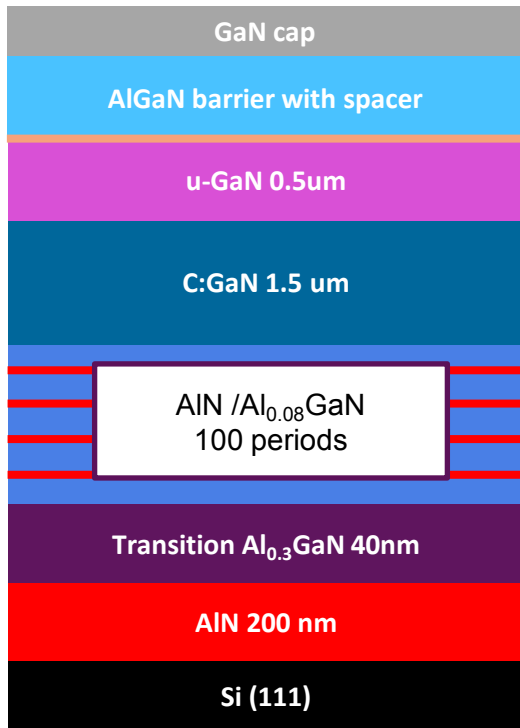


# Substráty pro heteroepitaxní růst GaN

Property	GaN	Si	Sapphire	SiC
Orientation	(0001)	(111)	(0001)	(0001)
Lattice mismatch GaN/substrate (%)	-	-15	+16	+3.5
Thermal mismatch GaN/substrate (%)	-	+55	-26	+33
Thermal conductivity ( $W/cm.K$ )	2.3	1.5	0.5	4.9
Max. wafer size availability ( $mm$ )	50	300	200	150
Cost	Prohibitive	Low	Medium	High



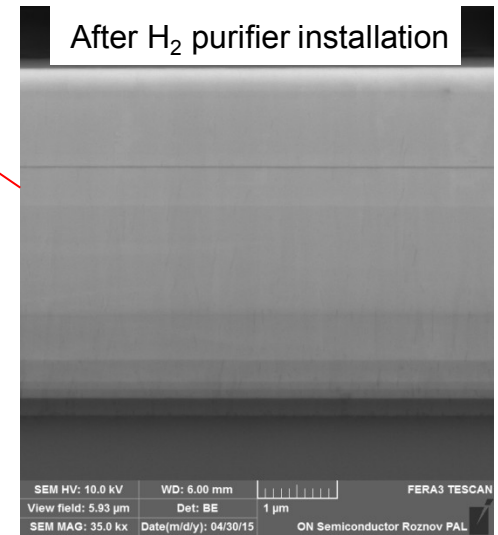
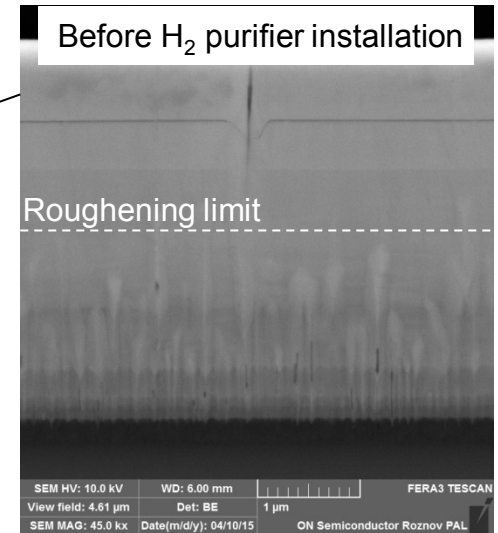
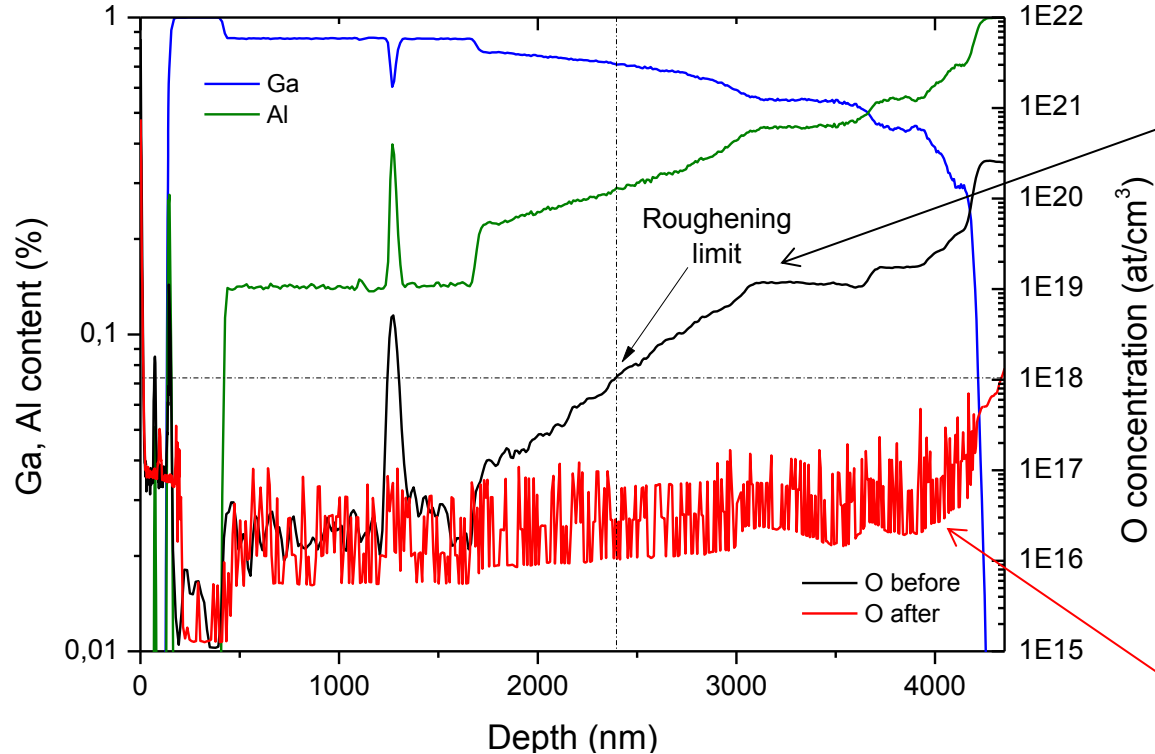
# Supermřížky pro heteroepitaxní růst



Defects originating from localized low AIN quality

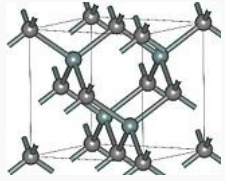
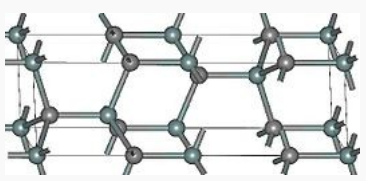
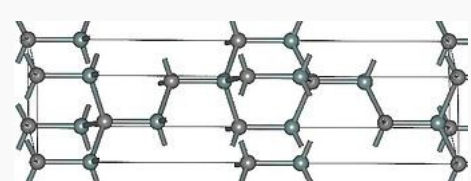
Dislocation blocking At SLS / GaN interface

# Vliv kontaminace kyslíkem



- **Defect formation due to the oxygen contamination:**

- Formation of inversion domains on the oxidized Si surface.
- Low AlN quality and coalescence due to oxidation of the material during growth.
- Localized Ga-Si melt-back etching due to Ga diffusion through the defects in the AlN layer.

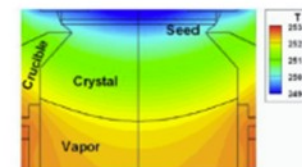
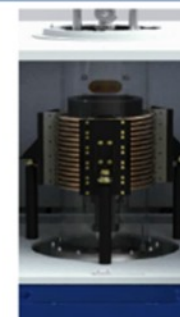
Polytyp:	( $\beta$ )3C-SiC	4H-SiC	( $\alpha$ )6H-SiC	Křemík	GaN
Krystalová truktura					
Šířka pásu zak. en. [eV]	2.2	3.26	3	1.1	3.39
Elektr. pohyblivost [cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> ]	900	1140 ( <i>//c</i> )	370 ( <i>//c</i> )	1350	900
Kritické el. pole [MV/cm]	1.2	3	2.4	0.3	3.3
Tepeňá vodivost [W.cm <sup>-1</sup> .K <sup>-1</sup> ]	4.9	4.9	4.9	1.5	1.3

# SiC - růst objemových krystalů

- Sublimace prášku
- Depozice z plynné fáze na zárodečnou desku
- Procesní teplota 2200 – 2400 °C
- Rychlost růstu 0.3 – 0.8 mm/
- 3 - 4 dny/běh
- délka krystalu 2 - 3 cm

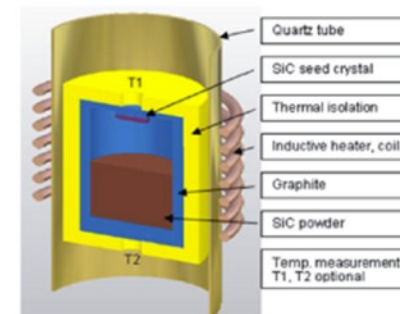
PVA TePla

Crystal Growing Systems  
baSiC-T, High temperature processes for silicon carbide



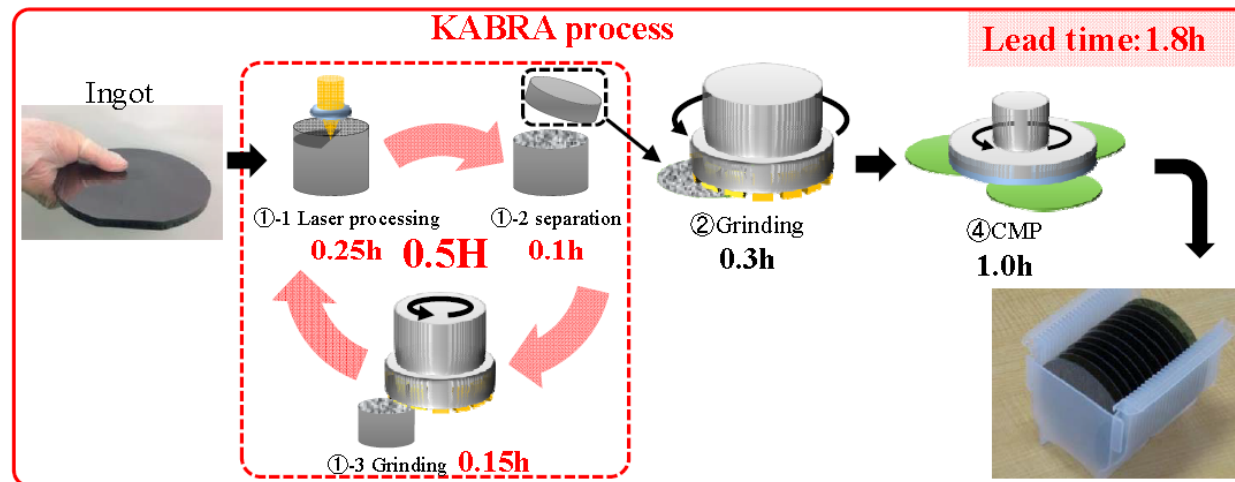
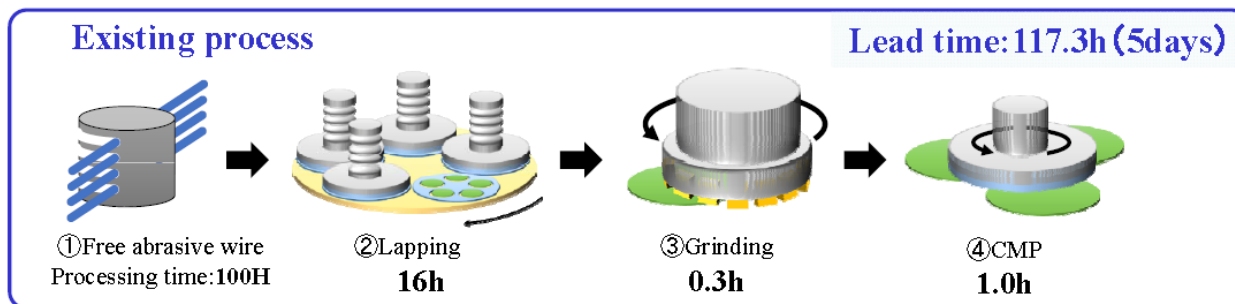
Crystal shape and temperature distribution in the growth chamber after the growth.

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# SiC - výroba desek

- Principiálně podobná křemíku
- Velice tvrdý materiál
  - ⇒ pomalé procesy
  - ⇒ dedikovaná zařízení



# Vývoj nových analytických metod



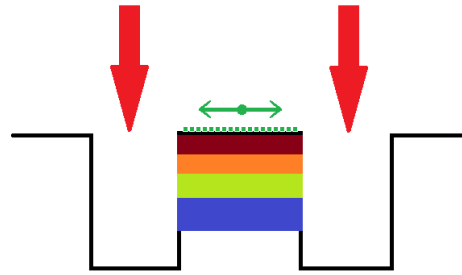
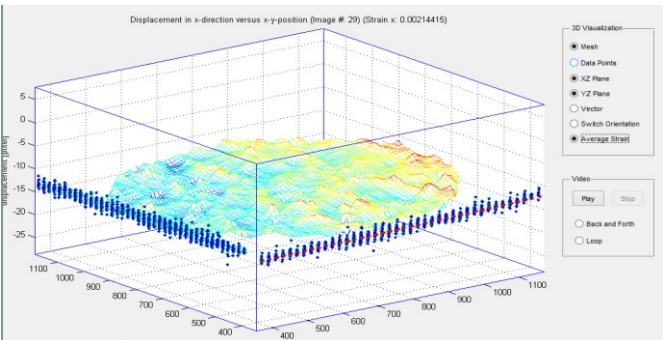
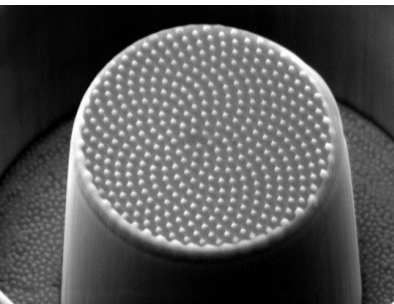
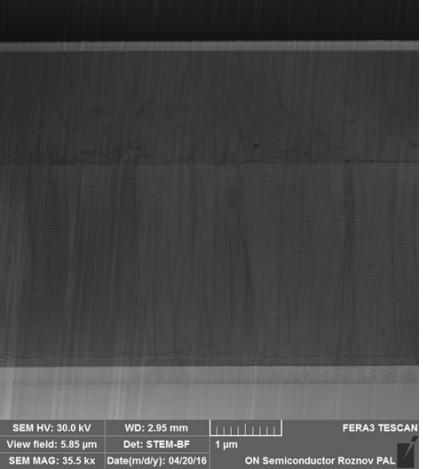
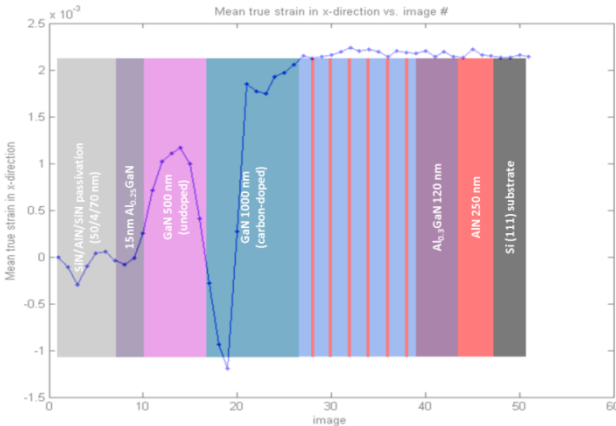
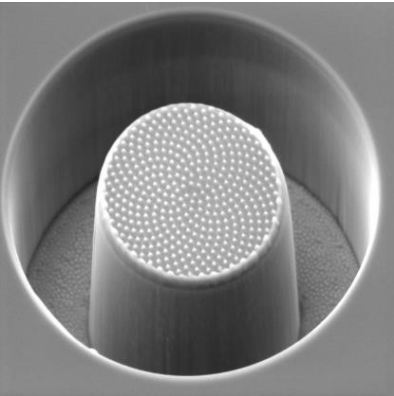
# Installed prototype of Plasma Xe FIB SEM



FERA3 GM Xe Plasma FIB SEM (STEM, EDX, mono GIS: XeF<sub>2</sub>, W, SiO<sub>2</sub>), installed and operated since 12/2014 in ON SEMICONDUCTOR.

# Methods for analysis of semiconductors with Plasma Xe FIB-SEM

- Demonstration of stress analysis in GaN(Al)N/Si structure with Ga FIB and STEM for R&D of Ga(Al)N layered structure incl. AlGaN/AlN superlattice (with requested nano-scale resolution).

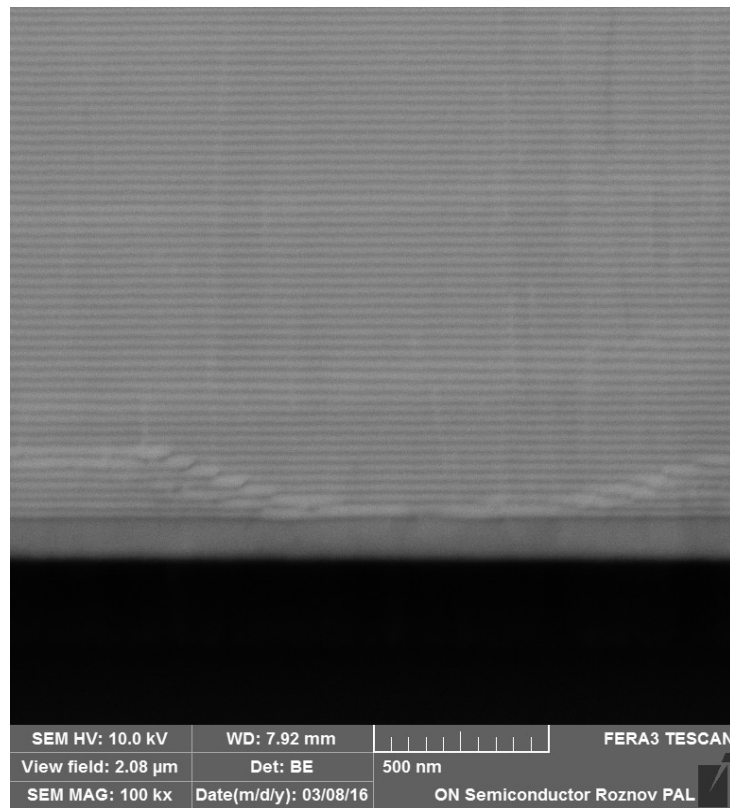
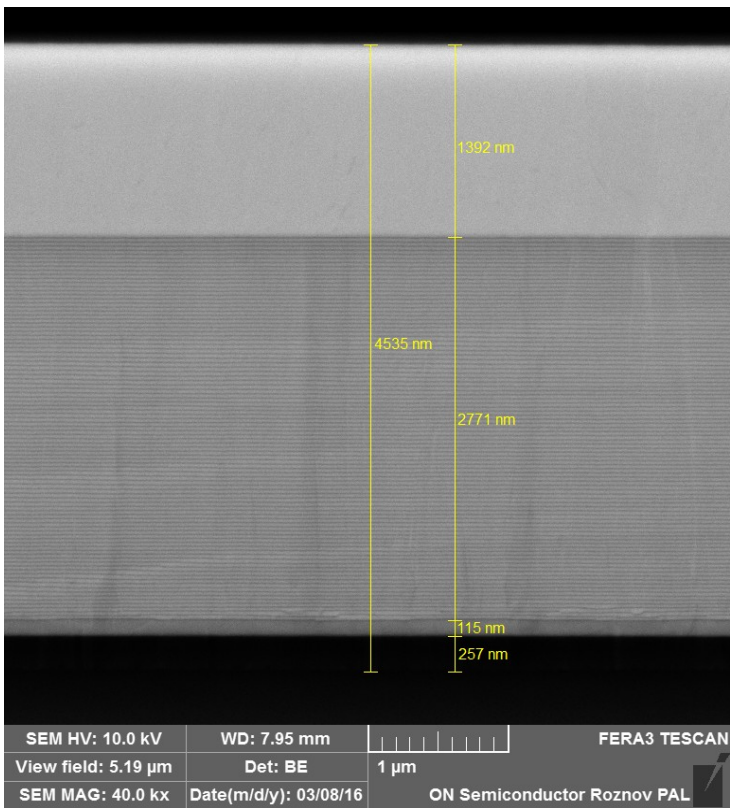


- The method for internal stress evaluation with FIB is a topic and result of different iSTRESS project. Our work is involved in the application on semiconductor structures and for utilization of Xe iFIB.



# SEM imaging - BE

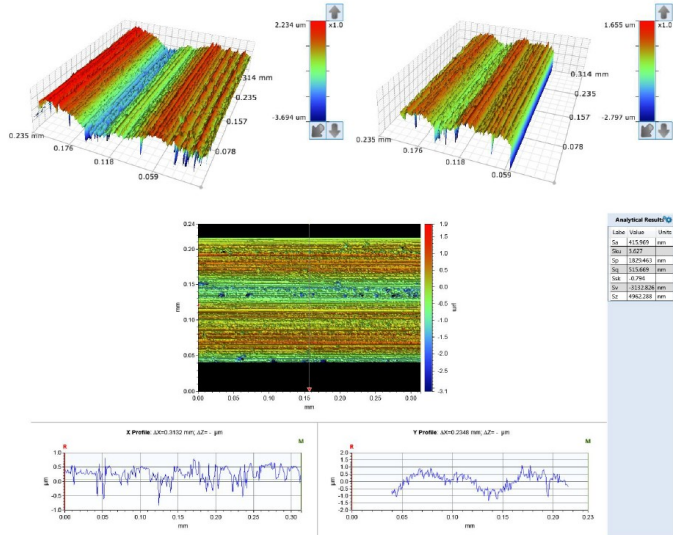
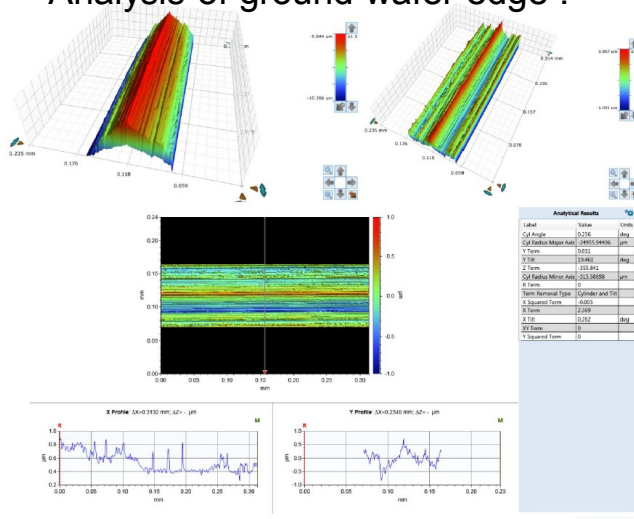
SEM(BE) of heteroepitaxial superlattice (SL) of AlGa<sub>N</sub> and AlN, which is used for growth of HEMT structures on Si substrate. SL is strained-layer structure that could stop dislocation propagation from the substrate-layer interface. 30 regular analysis of Ga(Al)N/Si structures were completed in 2016.



# Characterization of wafers flatness and topography

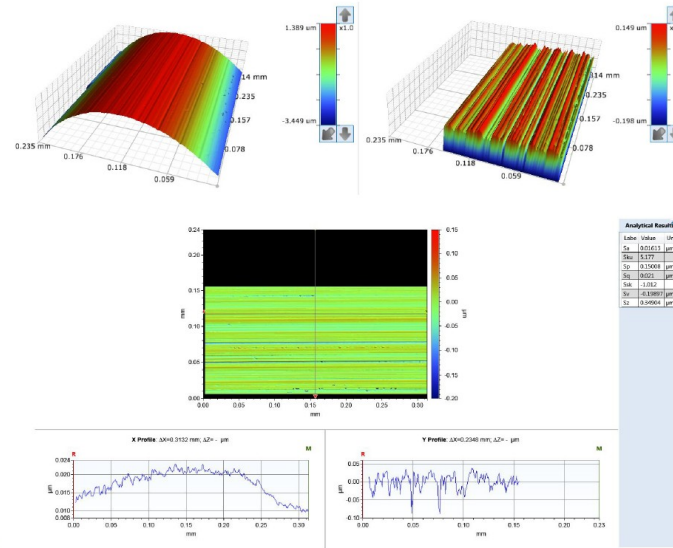
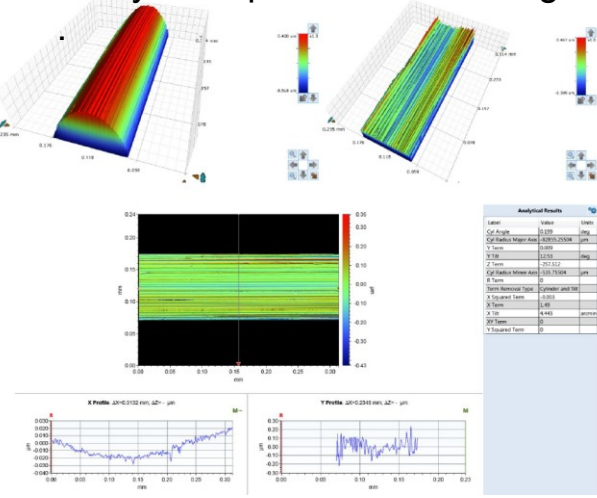
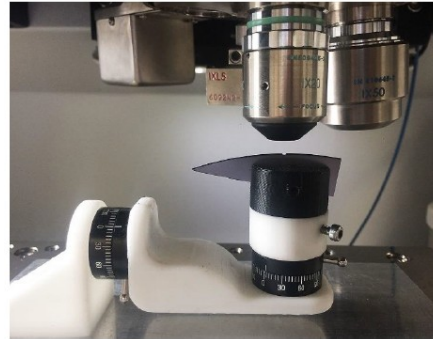
Optical Tribomometer  
Contour GT X8 Bruker.

Analysis of ground wafer edge .



Analysis of polished wafer edge

Analysis of Si wafer.



# Závěr

- Představený úvod je pouze malou částí využití fyziky v polovodičových procesech
- Fyzika pevných látek
- Fyzikální chemie
- Fyzika polovodičových součástek
- Fyzikální aplikace polovodičových součástek