FC250 Nano- and microtechnologies
chapter 1. Introduction

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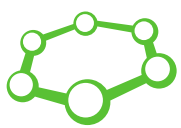

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Outline - chapter 1. Introduction

- 1.1 Fields of Expertise, Suggested Literature
- 1.2 Approaches in Micro/Nanotechnologies
- 1.3 Overview of Top-Down Fabrication
- 1.4 Plasma Technologies
- 1.5 Examples of Bottom-Up Fabrication
- 1.5 Fabrication of micro- and nanodevices

1.1 Fields of Expertise, Suggested Literature

Nanotechnology definition:

- Any technology on a nanoscale that has applications in the real world. (*from Handbook of Nanotechnology*)
- Research and technology development at the atomic, molecular, or macromolecular levels, in the length scale of approx. 1–100 nm range, to provide a fundamental understanding of phenomena and materials at the nanoscale and to create and use structures, devices, and systems that have novel properties and functions because of their small and/or intermediate size. The novel and differentiating properties and functions are developed at a critical length scale of matter typically under 100 nm. (*after National Science and Engineering Technology Council NSET, Feb 2000,* `www.nsf.gov/crssprgm/nano/reports/omb_nifty50.jsp`)

What Expertise is Necessary?

Material processing requires knowledge of processes:

- **gas kinetics** (for processes from vapor/gas phase)
- **film growth** (general views like adsorption, desorption, utilization etc.)
- **interaction of ions with solid** (for ion beam and plasma techniques)
- **chemistry** (for chemical and plasmachemical methods)
- **plasma-related phenomena**, i.e. plasma physics, principles of electrical discharges, elementary processes in plasma, plasma-surface interation

The processes often takes places at decreased pressure. Therefore, a knowledge of **vacuum technology** is also required.

This information are then applied to master the **material processing techniques**:

- **etching** (physical sputtering, chemical etching, plasma etching)
- **vacuum evaporation** for thin film deposition
- **magnetron sputtering** for thin film deposition
- **chemical vapor deposition** (CVD)
- **plasma enhanced chemical vapor deposition** (PECVD)
- etc.

Handbooks of Technologies

- Handbook of Thin-Film Deposition Processes and Techniques, ed. K. K. Schuegraf, Noyes Publications 1988
- Handbook of Plasma Processing Technology (Fundametals, Etching, Deposition, and Surface Interaction), ed. S. M. Rossnagel, J. J. Cuomo a W. D. Westwood, Noyes Publications 1989
- Handbook of Ion Beam Processing Technology (Principles, Deposition, Film Modification and Synthesis), ed. J. J. Cuomo, S. M. Rossnagel, H. R. Kaufman, Noyes Publications 1989
- Handbook of Thin Film Deposition Techniques (Materials and Processing Technology), by Krishna Seshan, (Noyes Publications 2002)
- Handbook of Plasma Immersion Ion Implantation and Deposition, Wiley 2000
- **Handbook of Nanotechnology (Springer 2010), B. Bushan**

Books Focused on Specific Processes and Technologies

- Thin Films Phenomena, K. L. Chopra, McGraw-Hill 1969
- **Thin-Film Deposition, Principles and Practice by Donald L. Smith, McGraw-Hill, 1995**
- Chemical reactor, analysis and design, G. F. Froment and K. B. Bischoff, John Wiley 1990
- Ion-Solid Interactions, Fundamentals and Applications, M. Nastasi, J. W. Mayer and J. K. Hirvonen, Cambridge University Press 1996
- Principles of plasma discharges and materials processing, M. A. Lieberman and A. J. Lichtenberg, John Wiley 1994
- **Lecture notes on principles of plasma processing, F. F. Chen and J. P. Chang, Kluwer Academic 2003**

Books focused on Specific Materials

- Tribology of Diamond-like Carbon Films: Fundamentals and Applications, by Christophe Donnet and Ali Erdemir, Springer, 2008
- Carbon Nanotubes: Science and Applications, M. Meyyappan ed., CRC Press 2004
- The Science and Technology of Carbon Nanotubes, K. Tanaka, T. Yamabe, F. Fukui eds., Elsevier 1999
- Nanostructures & Nanomaterials: Synthesis, Properties & Applications by Guozhong Cao, Imperial College Press, 2004

Scientific Papers

There are several electronic information resources `http://knihovna.sci.muni.cz/`:

- databases of scientific publications that collect information independently on the publisher and often contain links to full texts
  - Web of Science
  - Scopus
  - INSPEC
- databeses of scientific publications from given publisher - always connected with full texts but the download must not be for free (depends on the institutional domain, e. g. sci.muni.cz), some journals are “open access” (authors pay for the publication)
  - Science Direct
  - IOPscience
  - PROLA

Related courses

- F7360 Characterization of surfaces and thin films (in English, spring semester 2018)
- FB100 Plasmachemical processes (in English, fall semester)
- F3390 Micro- and nano-structures preparation (spring semester)
- F4280 Thin Films Deposition and Surface Modification Technologies (spring semester)

1.2 Approaches in Micro/Nanotechnologies

1.2 Approaches in Micro/Nanofabrication

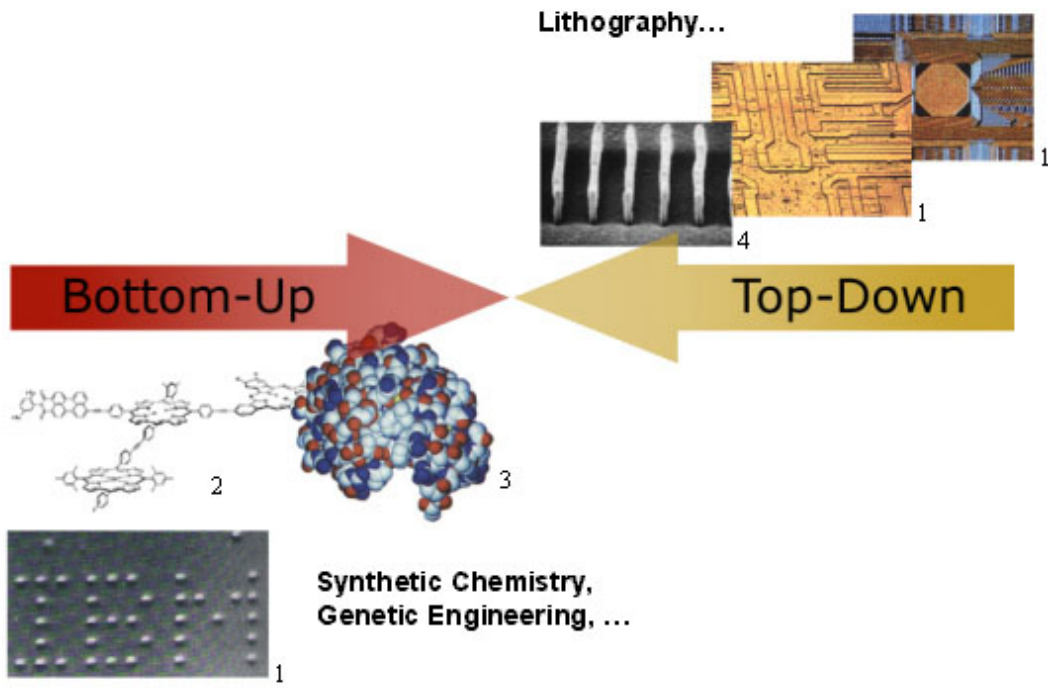
Two principle approaches can be used for micro/nanofabrication:

top-down approach:

- deposition of thin films
- doping
- etching/sputtering (lithography, i.e. through a mask, and nonlitographic fabrication)
- preparation of surfaces (cleaning, polishing, functionalization)

bottom-up

- building using nanoobjects (atoms, molecules),
- self-assemply of structures



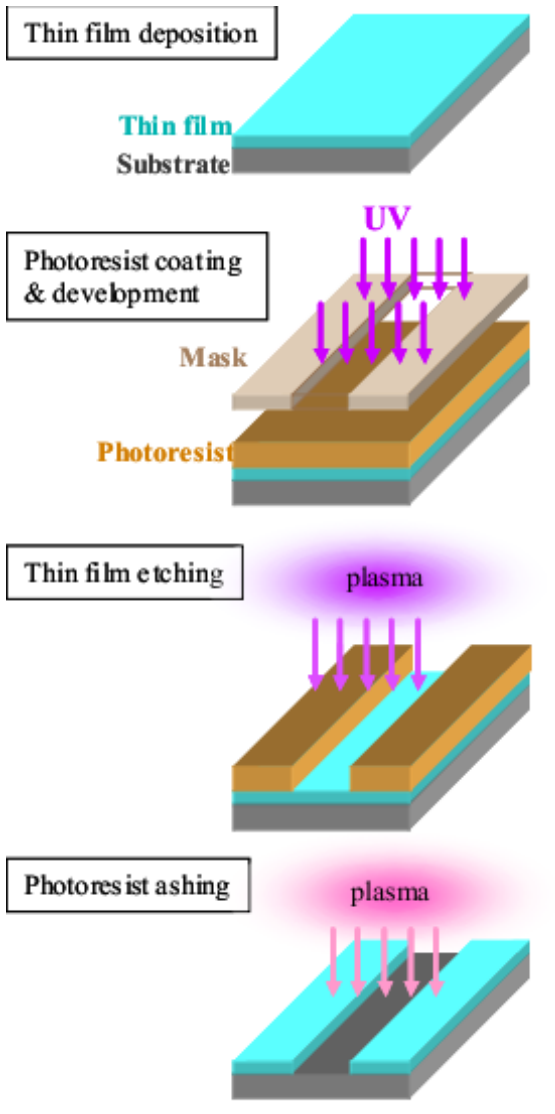
1.3 Overview of Top-Down Fabrication

- Lithography
- Etching/Sputtering Processes
- Preparation of Films
- Doping
- Surface Treatment

Basics of Lithography

Microlithography is a technique that creates microstructures after given geometrical template:

- Lithography is usually applied to shape a thin film $\Rightarrow$ deposition of thin film
- Photosensitive material (resist) is coated on the material that should be shaped
- Resist is irradiated through a mask, by projection of UV image or by directed electrons (photolitography or electron lithography)
- Resist development:
  - positive resist: soluble in developper at the irradiated places
  - negative resits: unsoluble in developper at the irradiated places
- Etching of the film through photoresist pattern
- Rest of the resist is removed



lithography patterning with positive resist

Etching/Sputtering Processes

ion sputtering

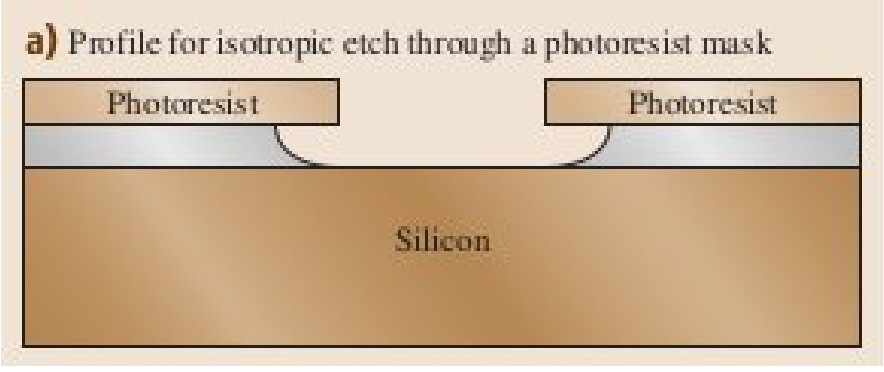
- purely physical approach, removal by energy transfer
- slow process, no selectivity
- ions are directed by electric field, i.e. anisotropic process

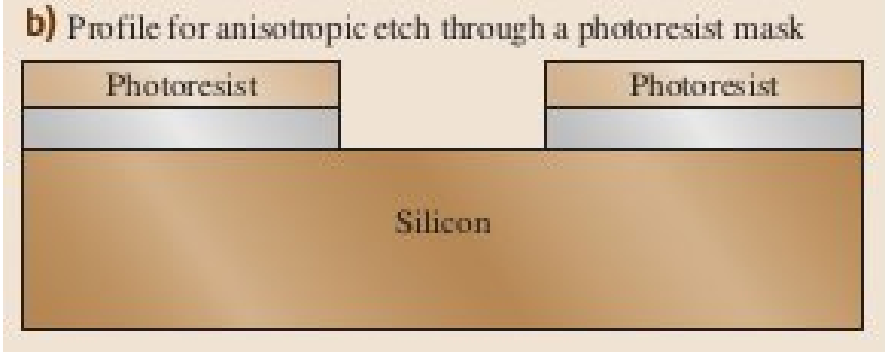
chemical etching

- purely chemical processes that requires aggressive chemicals and/or elevated temperature for reaction activation
- can be very fast, selective
- chemical reactions with surface are not directed, i.e. isotropic process

plasma etching

- combination of physical and chemical approaches
- directional process





Preparation of Films

Difference between thin-film and thick-film technology:

- thin-film technology: deposition of individual molecules, film thickness 10 nm–10 μm
- thick-film technology: involves deposition of particles (e.g. painting, silk screening, spin-on-glass coating, plasma spraying)

Several aspects have to be taken into account:

- functional properties of the deposition
- uniformity of the processes
- step coverage
- conformality
- reproducibility
- simplicity
- price
- etc.

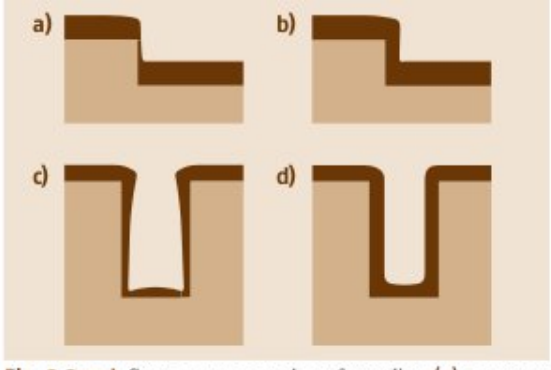


Fig. 8.3a–d Step coverage and conformality: (a) poor step coverage, (b) good step coverage, (c) nonconformal layer, and (d) conformal layer

Thin-Film Process Steps

All thin-film processes contain the four (or five) sequential steps.

1. A **source** of film material is provided.
   Solid, liquid, vapor or gas source. Solid materials need to be vaporized (by heat or energetic beam of electrons, photons, i.e. laser ablation, or positive ions, i.e. sputtering) - **physical vapor deposition (PVD)**. The methods using gases, evaporating liquids or chemically gasified solids are **chemical vapor deposition (CVD)** methods.
2. The material is **transported** to the substrate.
   The major issue is uniformity of arrival rate over the substrate area. Transport in a high vacuum = straight travelling lines $\rightarrow$ importance of geometry. Transport in a (gaseous) fluid = many collisions $\rightarrow$ gas flow patterns, diffusion of source molecules through other gases present.
3. The film is **deposited** onto the substrate surface.
   It is influenced by source and transport factors and the conditions at the deposition surface. Three principal surface factors: (i) surface condition (roughness, contamination, degree of chemical bonding with the arriving materials and crystallographic parameters in the case of epitaxy), (ii) reactivity of arriving material (sticking coefficient S_c from 1 to less than 10^{-3}) and (iii) energy input (substrate heating, photons, ions, chemical energy).

Thin-Film Process Steps

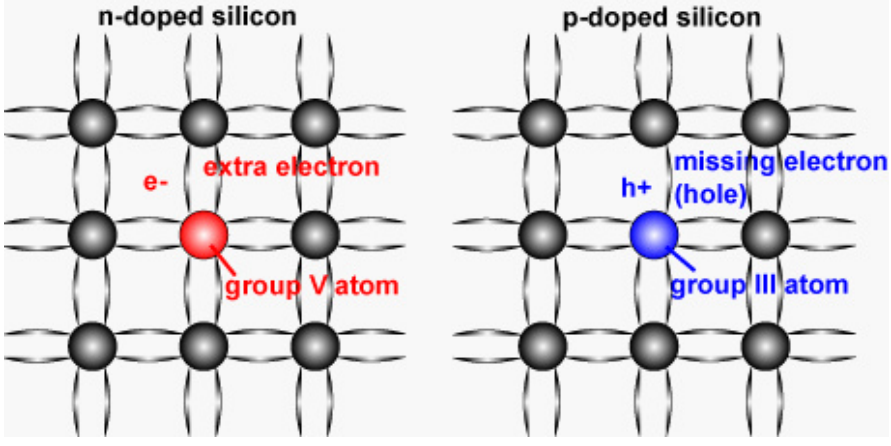
4. (Optionally, **annealing** takes place)
5. The final step is **analysis** of the film.
   One level of analysis is the determination of functional properties important for given application and optimization of the deposition process for these processes (emphirical approach). A deeper level of analysis involves probing the film structure and composition (better understanding of the overall processes).

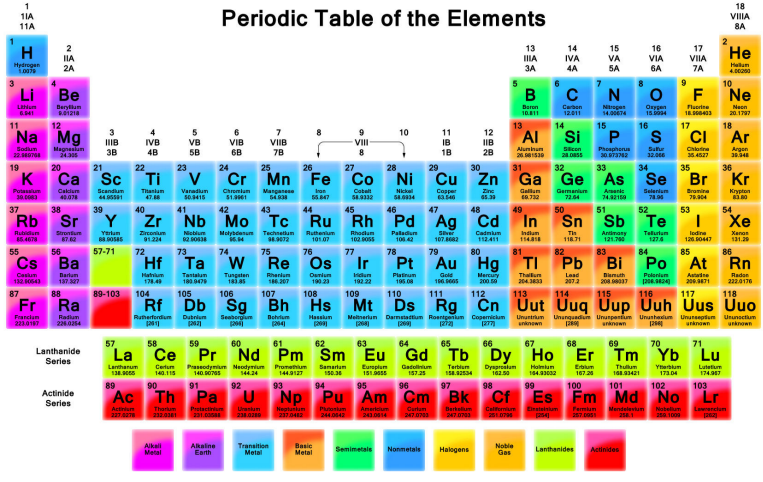
Analysis of the films after deposition - kind of final process monitoring. However, **monitoring** is important in all steps!

Doping

. . . process of introducing impurity atoms into a semiconductor region in a controllable manner in order to define the electrical properties of this region.

- All electronic and optical semiconductor devices incorporate dopants as a crucial ingredient of their device structure.
- The doping with donors and acceptors allows to modify the electron and hole concentrations in Si in a very large range from 10^{13}cm^{-3} up to 10^{21}cm^{-3}.
- The carrier concentration can also be varied spatially quite accurately which is used to produce pn-junctions and built-in electric fields.





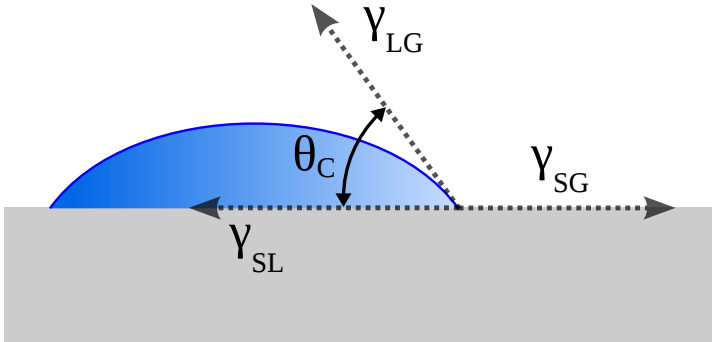
Surface Treatment

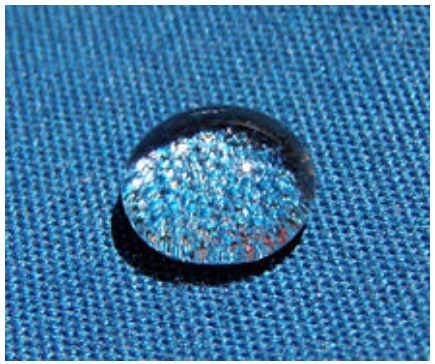
What can happen after surface treatment?

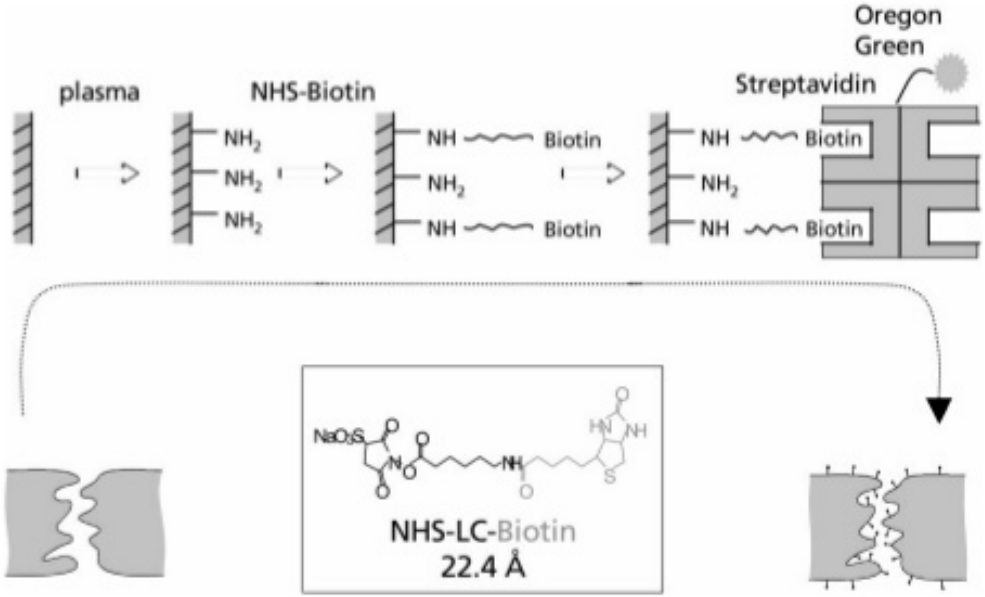
- change of surface roughness
- change of surface chemistry

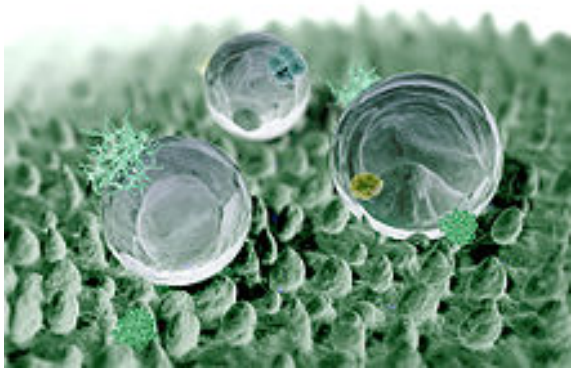
What can be these changes used for?

- change of surface free energy, i.e. wettability
- improved adhesion of further coatings
- immobilization of biomolecules









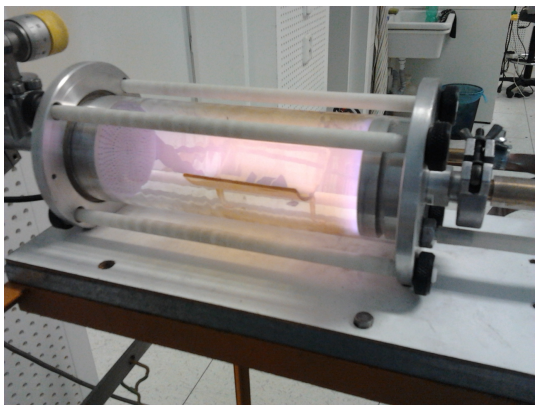
C. Oehr *et al.*, Surf. Coat. Technol. 116–119 (1999) 25–35

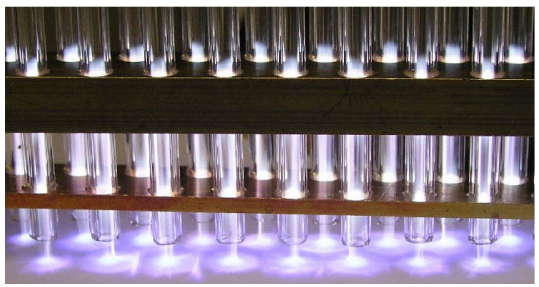
1.4 Plasma Technologies

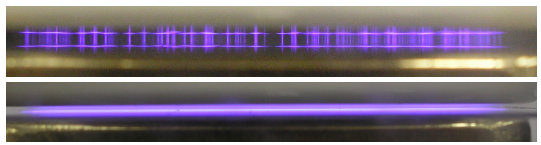
Unique Features of Plasma Technologies

Plasma of laboratory electrical discharge provides **environment of**

- **hot electrons** ($T \approx 10000$ K) $\Rightarrow$ dissociation of molecules into reactive species
- **positive ions** that can be accelerated by ≈ 100 eV near solid surface $\Rightarrow$ sputtering of targets, implantation, modification of surfaces and growing films
- **cold neutral gas** $\Rightarrow$ highly energetic process can be kept in a vessel, heat sensitive materials can be treated (e. g. polymers, even polymer nanofibers)







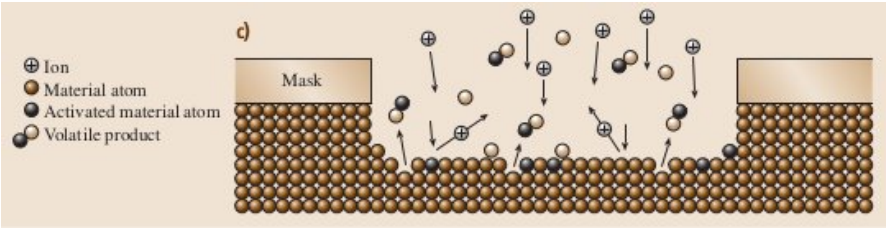
Plasma processing:

- is a dry process, i.e. with low consumption of chemicals,
- provides combined effect of physical processes (ions, UV photons), chemistry (radicals, excited species)
- offers replacement of toxic and explosive reactants
- enables preparation of new materials

Plasma Processing Methods

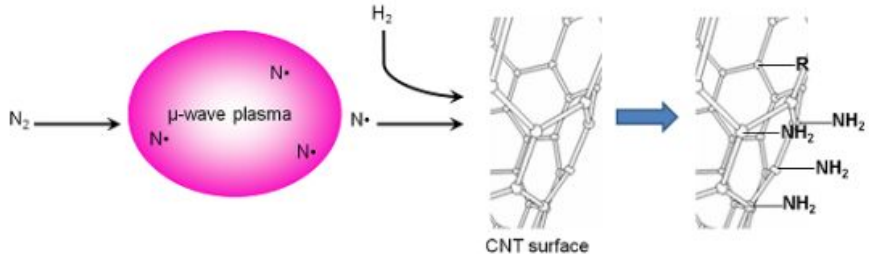
Plasma etching

anisotropic dry etching: combination of chemistry and effect of ions (reactive ion etching)



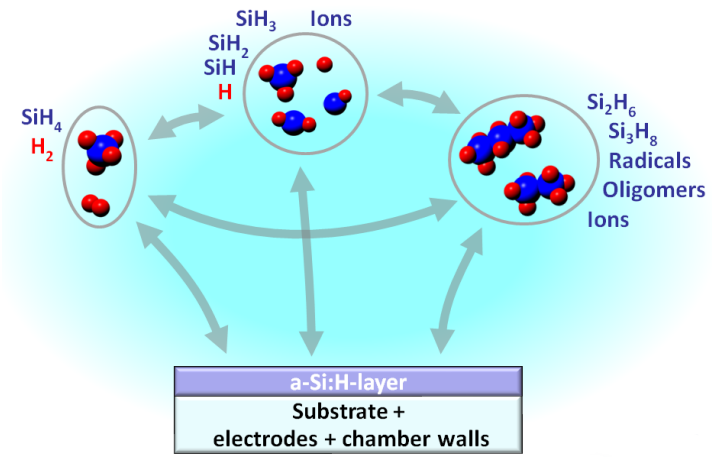
Plasma treatment in O_2, NH_3, CF_4 ...

creation of surface chemical group

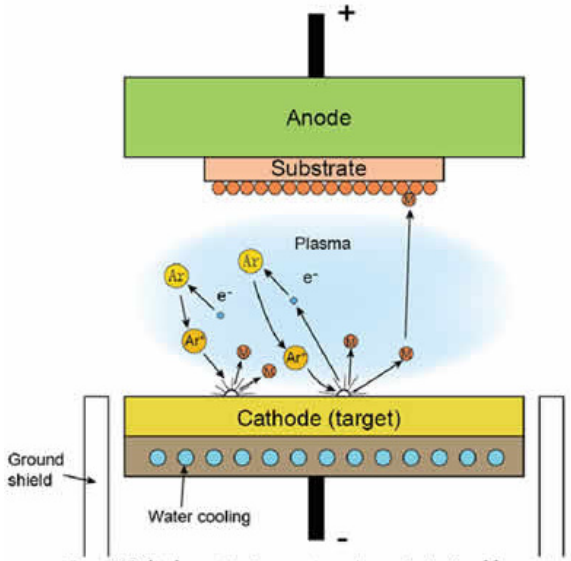


Plasma deposition of thin films

plasma enhanced chemical vapor deposition (PECVD)



physical vapor deposition (PVD) - dc diode sputtering, magnetron sputtering



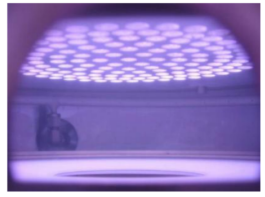
Commercial Plasma Reactors

Plasma reactors can also look very differently, like plastic boxes :-)

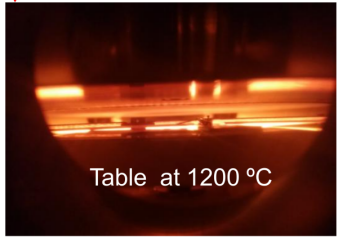
Oxford Instruments,
PlasmaPro 100
- **reactive ion etching**

Scalable and short process times:
- Sample size up to 8" wafer
- Load lock wafer handling

Plasma enabled CVD processes
- Choice of in-chamber or remote plasma (ICP) source



Flexible vapour delivery module for solids, liquid percursors
- Example: $Mo(CO)_6$,$MoCl_5$, $W(CO)_6$ for 2D MoS_2, WS_2 etc.



High temperature heated table

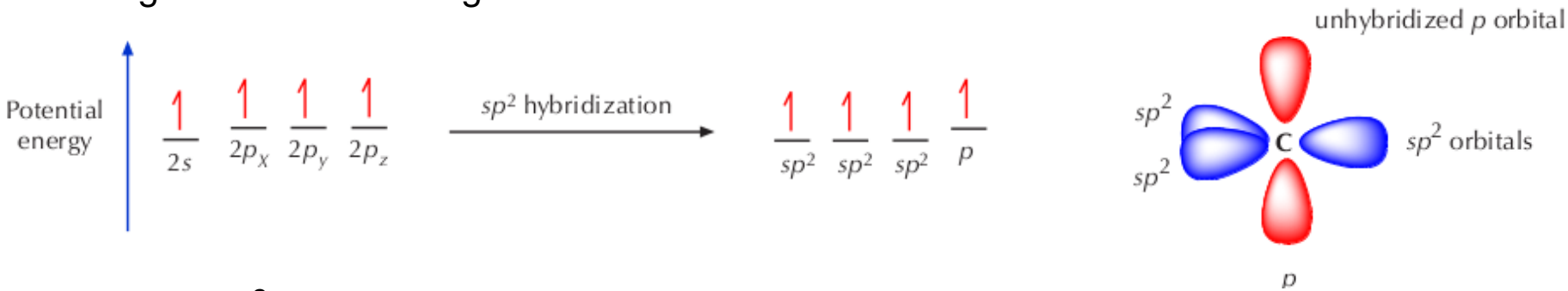
Oxford Instruments, NanoFab
- **high T (plasma enhanced) chemical vapor deposition** for deposition of carbon nanomaterials and other 2D materials

1.5 Examples of Bottom-Up Fabrication

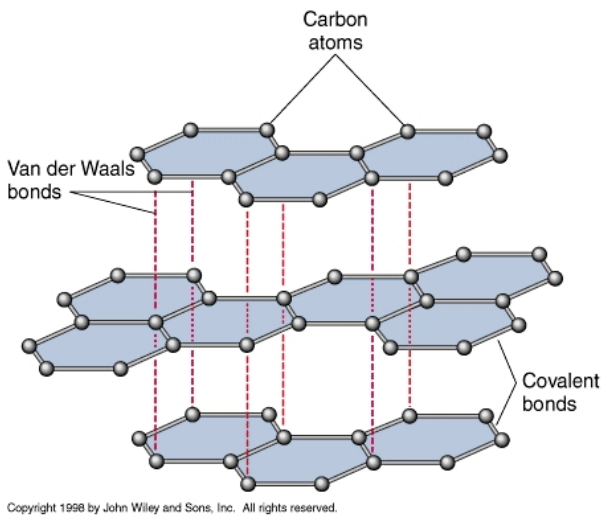
Carbon-Based Nanomaterials - formed by sp^2C

sp^2-C bonding (one valence electron in pure p state and the other three in hybrid orbitals) enables synthesis of several interesting carbon nanomaterials due to planar bond structure

Formation of 3 sp^2 hybrid orbitals: combination of 1/3s and 2/3p - trigonal planar bonding directions with angles of 120°

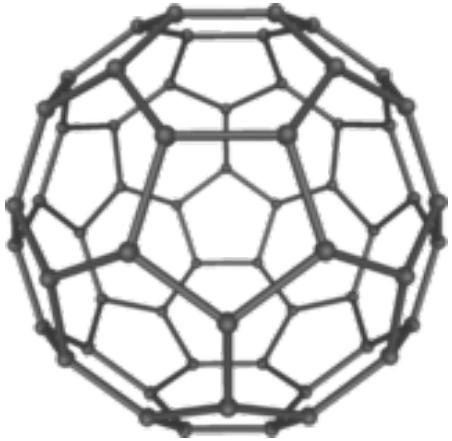


graphite, sp^2 bonded C



Carbon-Based Nanomaterials - formed by sp^2C

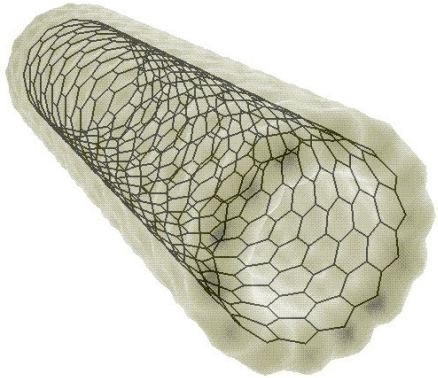
Fullerene - hollow sphere, ellipsoid *etc.*
Buckyballs - spherical fullerenes.



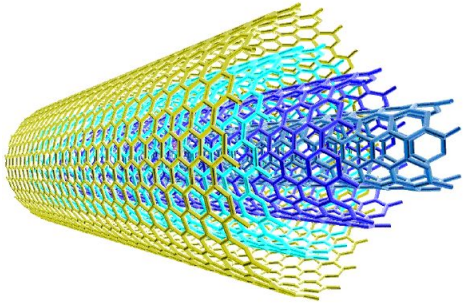
C60 - Buckminsterfuleren

prepared in 1985 at Rice University

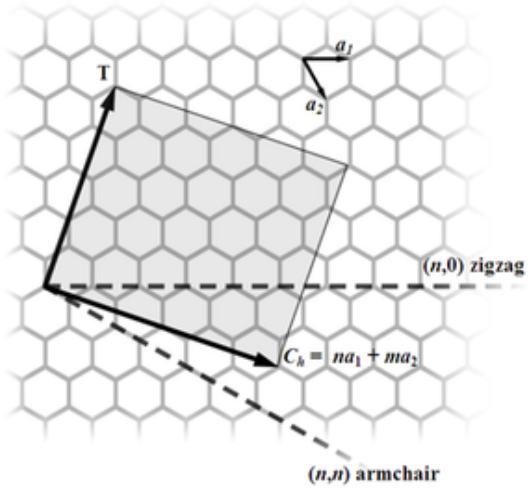
Single-walled carbon nanotube (SWCNT)

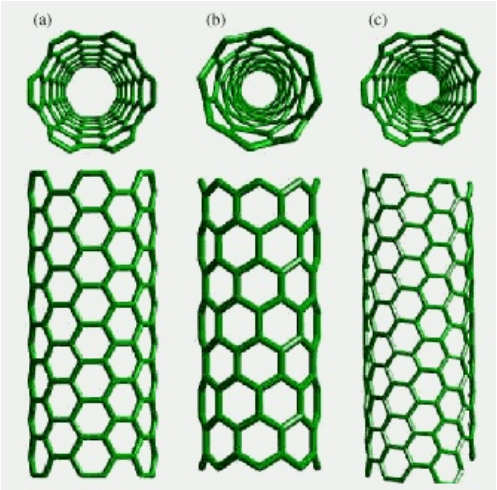


Multi-walled carbon nanotube (MWCNT)



- prepared 1991 by Iijima



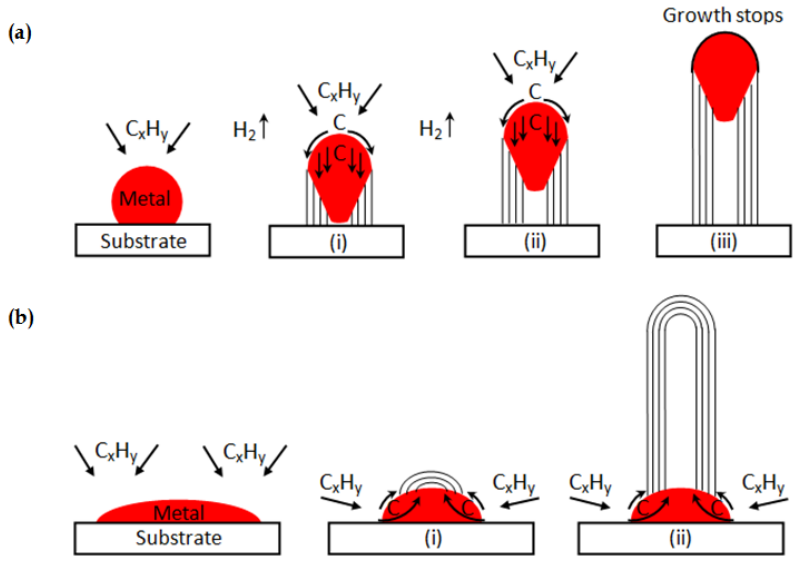


Different chirality of SWNT:

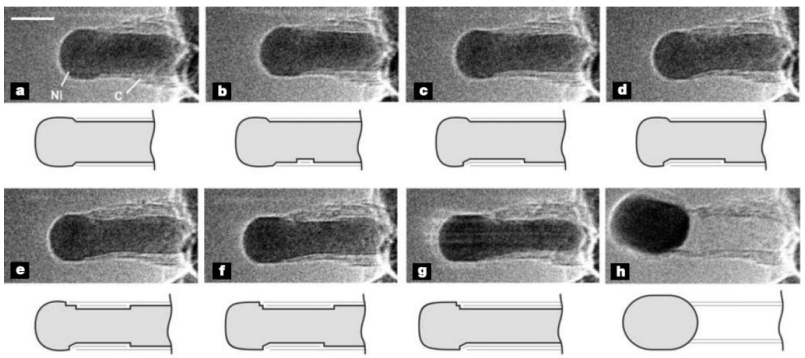
(a) armchair
(b) zigzag
(c) chiral (n,m)

Growth of Carbon Nanotubes

Widely-accepted growth mechanisms for CNTs: (a) tip-growth model, (b) base-growth model.



In situ HRTEM image sequence of a growing carbon nanofiber - images (a–h) illustrate one cycle in the elongation/contraction process.



Drawings are included to guide the eye in locating the positions of mono-atomic Ni step-edges at the graphene–Ni interface. Scale bar = 5 nm. (Helveg et al., 2004. Nature 427, 426-429)

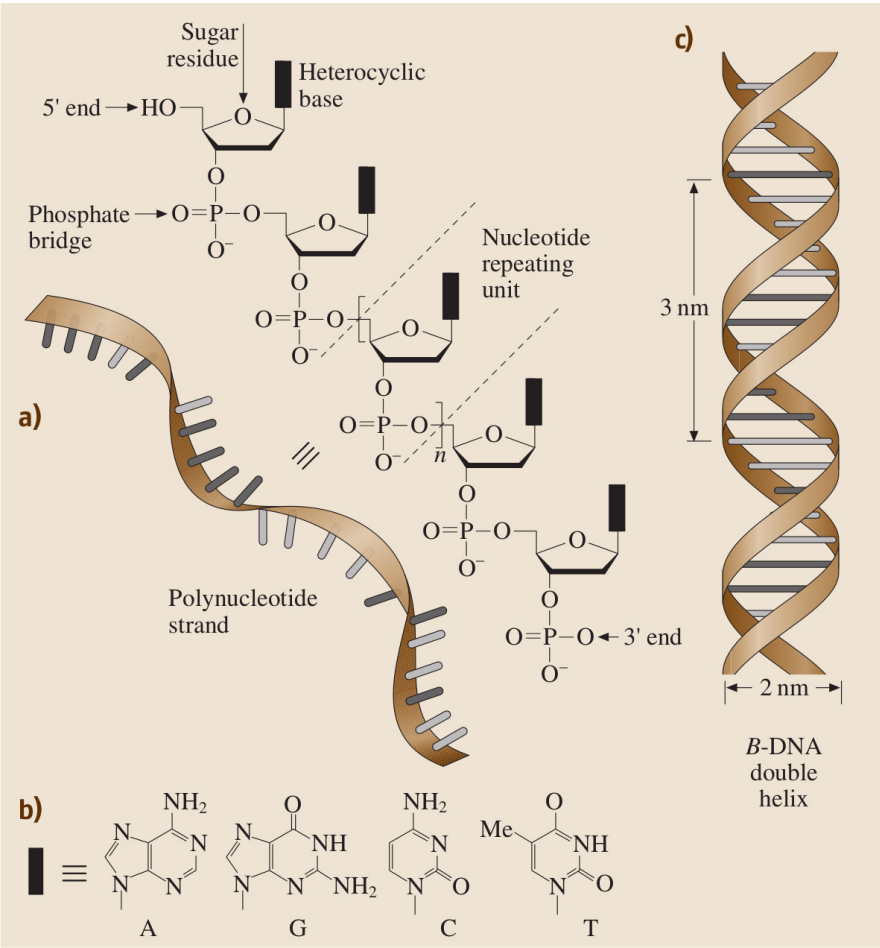
TEM video of growing CNTs

`https://www.youtube.com/watch?v=TaNCWcumeyg`

Mimicking Nature's Bottom-up Processes

Nature efficiently builds nanostructures by relying on chemical approaches:

- molecular building blocks: nucleic acids and proteins
- assembled in a variety of nanoscaled materials with defined shapes, properties, and functions.



example of **nucleic acids:**

- nucleic acids are large biomolecules (linear polymers) composed of **nucleotide repeating units** (Fig. a)
- nucleotides have 3 components: 5-carbon sugar, phosphate group, nitrogenous base.
- Chemical bonds between the phosphate of one nucleotide and the sugar of the next ensures the propagation of a polynucleotide strand from the 5' to the 3' end.

$\Rightarrow$ **main backbone of the polymeric strand**

- Every nucleotide carries **one of the four heterocyclic bases** shown in Fig. b.

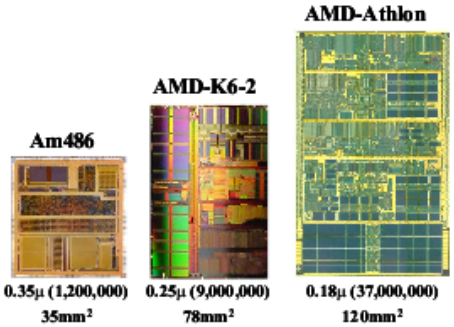
1.5 Fabrication of micro- and nanodevices

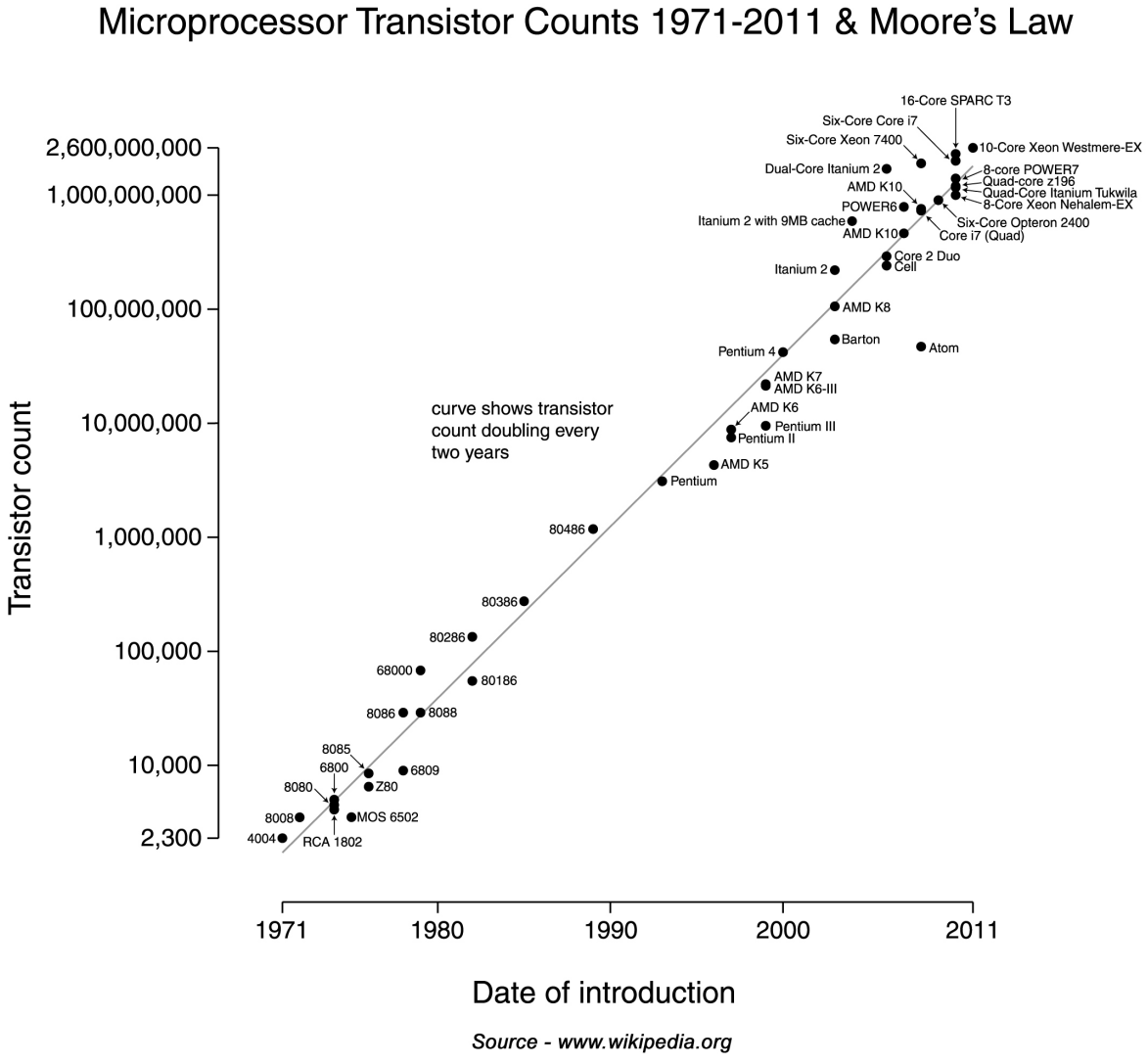
- Microelectronics - requires fabrication of integrated circuits (ICs)
- MEMS/NEMS - borrows standard methods from ICs and adds other processes

Microelectronics

Increase of integration:

- Small-Scale Integration (SSI) few transistors on chip,
- Medium-Scale Integr. (MSI) hundreds of transistors on chip (end of 60ties),
- Large-Scale Integration (LSI) 10 000 transistors on chip (70ties),
- Very Large-Scale Integr. (VLSI) 100 000 transistors on chip (begining of 80ties), 1 000 000 000 in 2007





Fabrication of Integrated Circuits

. . . multiple-step sequence of photolithographic and chemical processing steps during which electronic circuits are gradually created on a wafer made of pure semiconducting material. Silicon is almost always used, but various compound semiconductors are used for specialized applications.

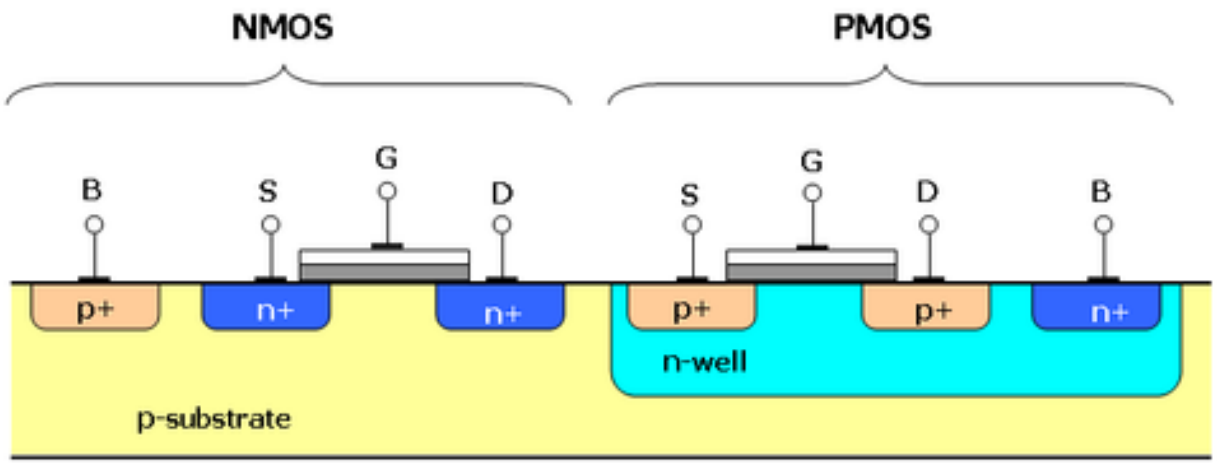
- **Front-end-of-line** (FEOL) is the 1st portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.
- **Back-end-of-line** (BEOL) is the 2nd portion of IC fabrication - individual devices (transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, the metalization layer (Cu, Al). BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.

Philips Chip Manufacturing Process
`https://www.youtube.com/watch?v=gBAKXvsaEiw` (start from 1')

Front-end-of-line (FEOL) Structure

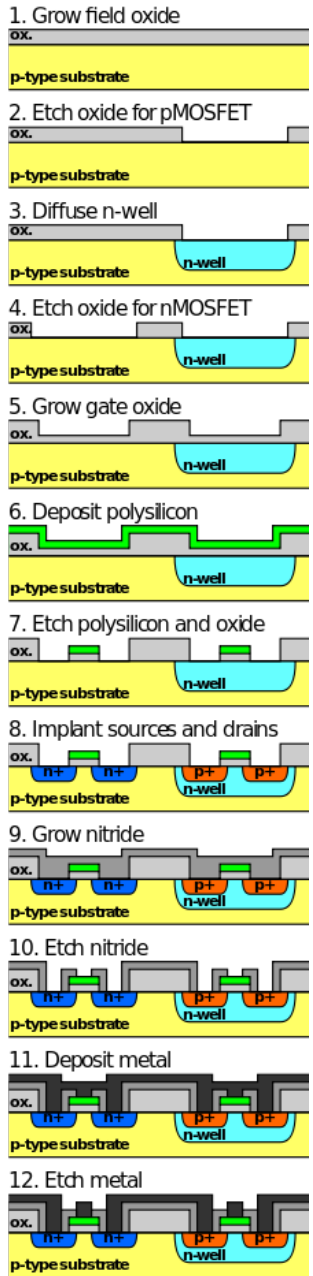
Today, **complementary metal-oxide-semiconductor** (CMOS) technology is the dominant semiconductor technology.

- uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

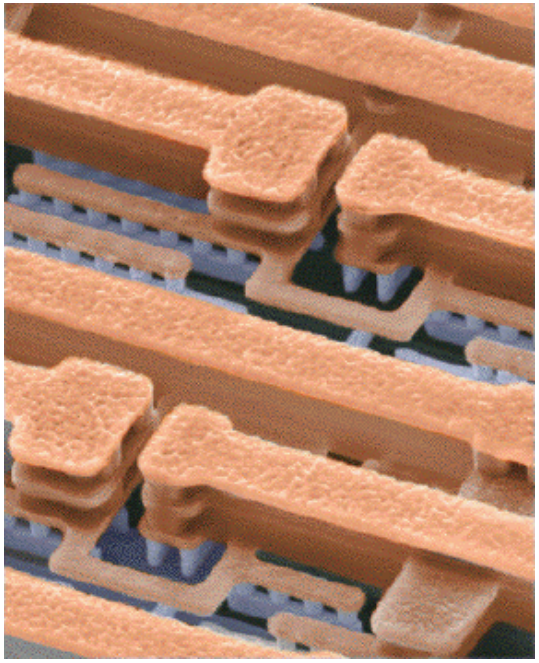


CMOS technology is used in microprocessors, microcontrollers, static RAM, and application specific integrated circuits (ASICs).

CMOS process flow
`https://www.slideshare.net/bhargavveepuri/cmos-process-flow`

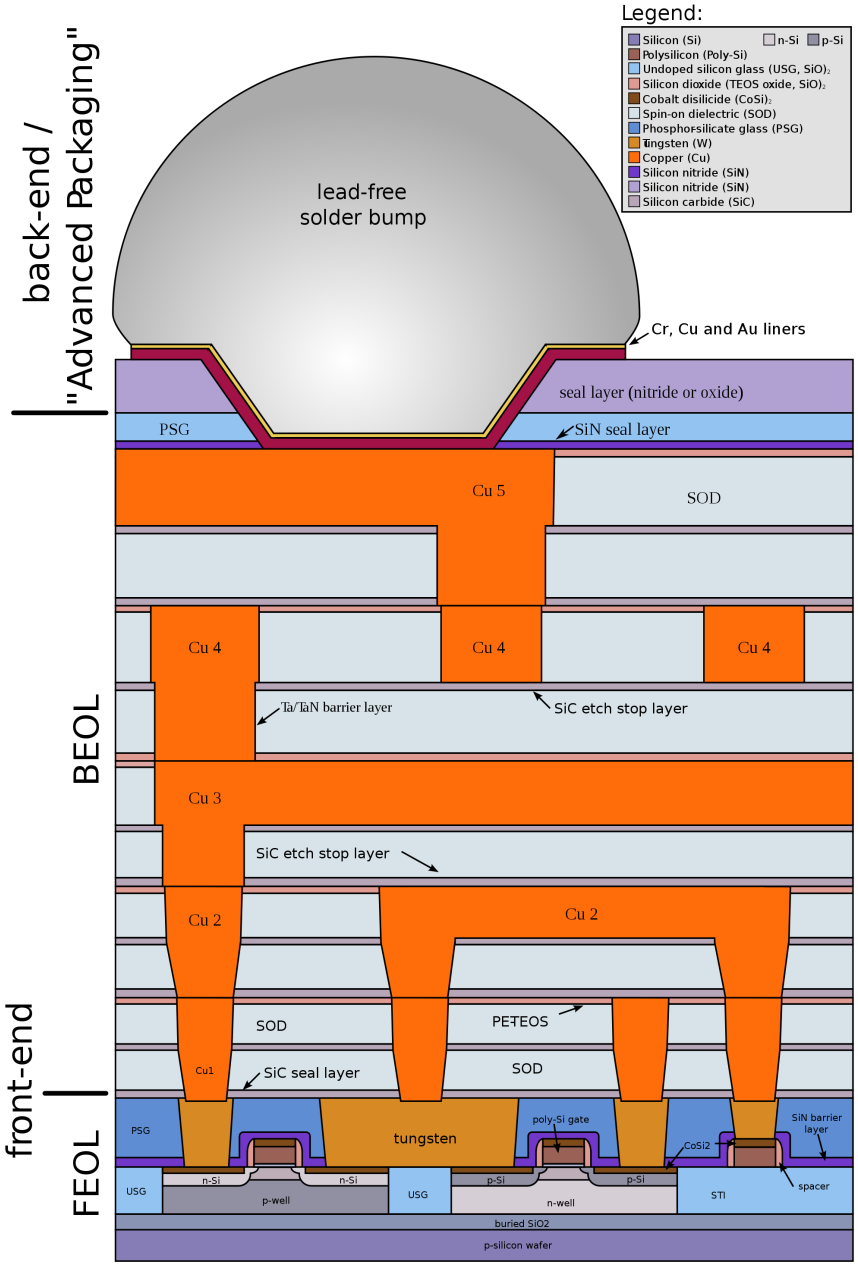


Back-end-of-line (BEOL) Structure



SEM view of three levels of copper interconnect metallization in IBM's CMOS integrated circuits

(Photograph courtesy of IBM Corp., 1997)



Technology Nodes in Microelectronics

Technology node - process sequence for manufacturing a chip

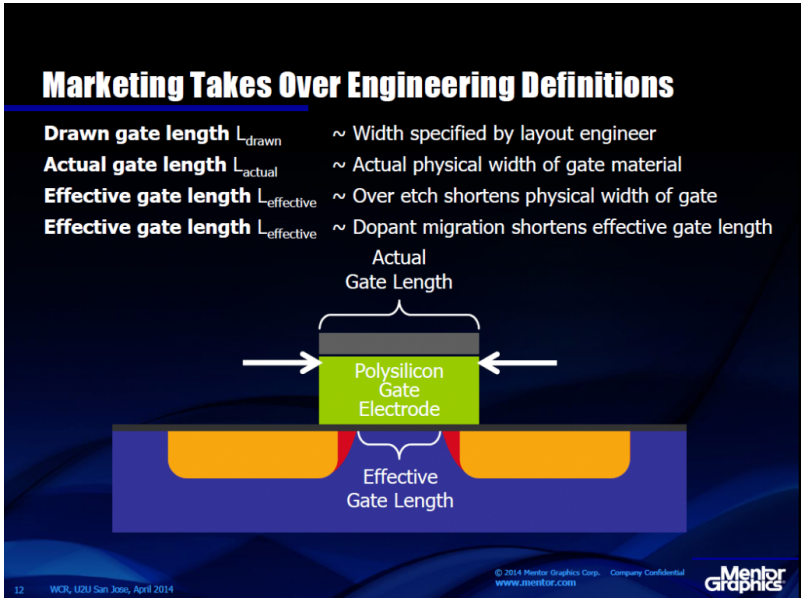
Pitch Counts

Year	Node	Half-pitch	Gate length*
2009 [a]	32	52	29
2007 [a]	45	68	38
2005 [b]	65	90	32
2004 [b]	90	90	37
2003 [b]	100	100	45
2001 [c]	130	150	65
1999 [c]	180	230	140
1997 [d]	250	250	200
1995 [d]	350	350	350
1992 [d]	500	500	500

* Here, gate width is defined as the physical gate length, which in recent years became smaller than the printed gate length.

[a] ITRS data 2008 update [b] ITRS data 2006 [c] ITRS data 2001 [d] ITRS data 1997

Note that each year skipped is identified on the ITRS as between nodes.



The device node - once equated to the half-pitch or spacing between the tightest metal lines then the minimum feature size in a chip and now a marketing term that continues to decrease linearly even if no feature on the chip can be found to match it.

What are MEMS/NEMS?

The acronym MEMS/NEMS (**micro / nanoelectromechanical systems**) originated in the USA. The term commonly used in Europe is microsystem technology (MST), and in Japan it is micro/nanomachines. Another term generally used is micro/nanodevices.

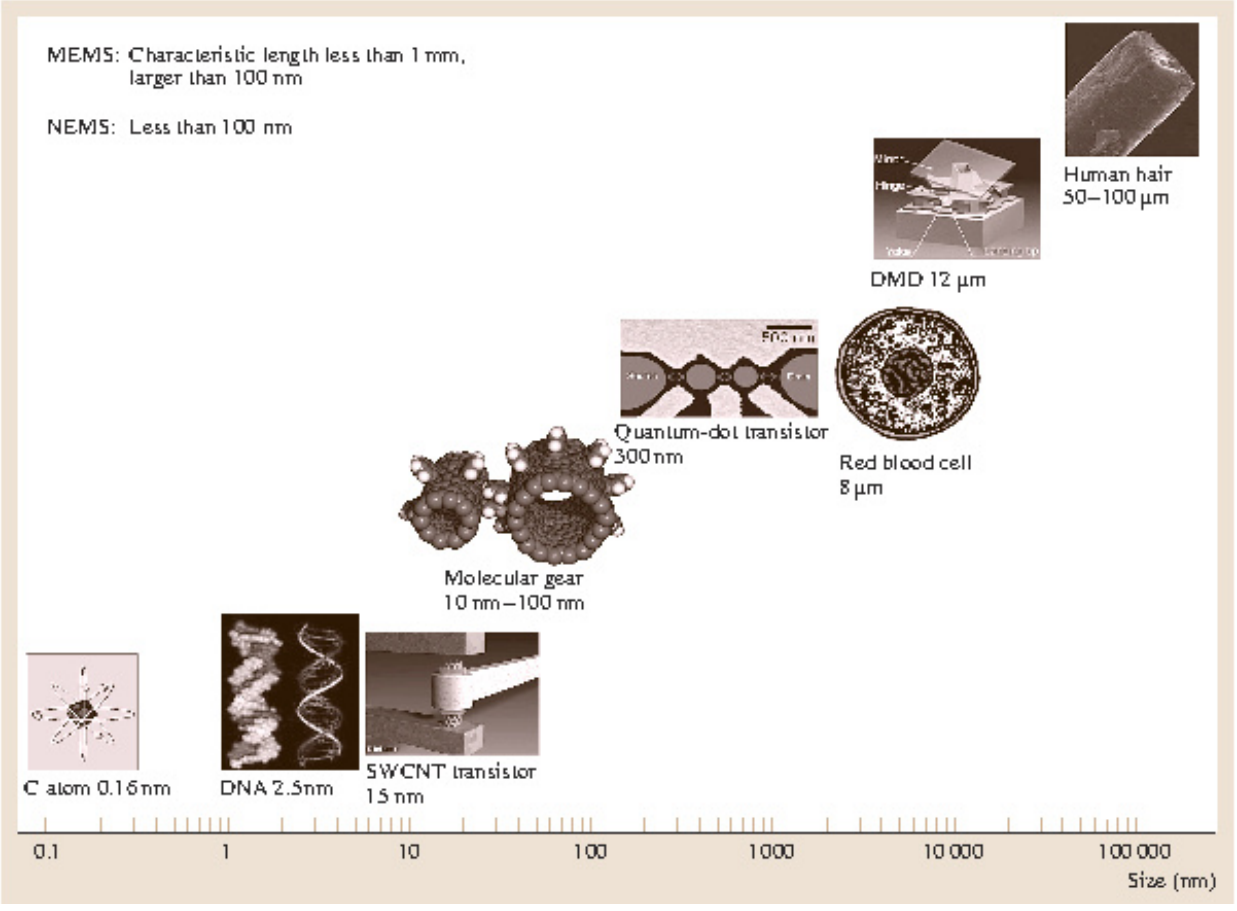
- MEMS - microscopic devices with characteristic length $< 1\,\text{mm}$ and $> 100\,\text{nm}$
- NEMS - nanoscopic devices with characteristic length $< 100\,\text{nm}$

MEMS/NEMS terms are also **now used in a broad sense** and include electrical, mechanical, fluidic, optical, and/or biological functions. They are referred to as intelligent miniaturized systems comprising e.g. sensing, processing and/or actuating functions.

MEMS/NEMS for

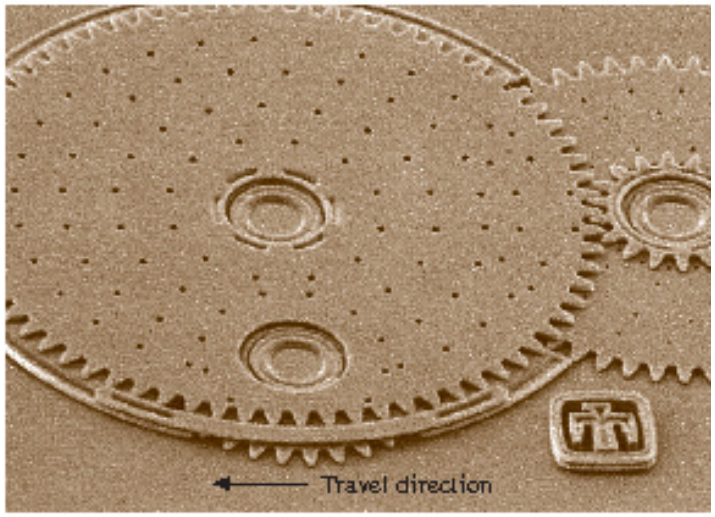
- optical applications -micro/nanooptoelectromechanical systems (MOEMS/NOEMS),
- electronic applications - radio-frequency-MEMS/NEMS or RF-MEMS/RF-NEMS.
- biological applications - BioMEMS/BioNEMS.

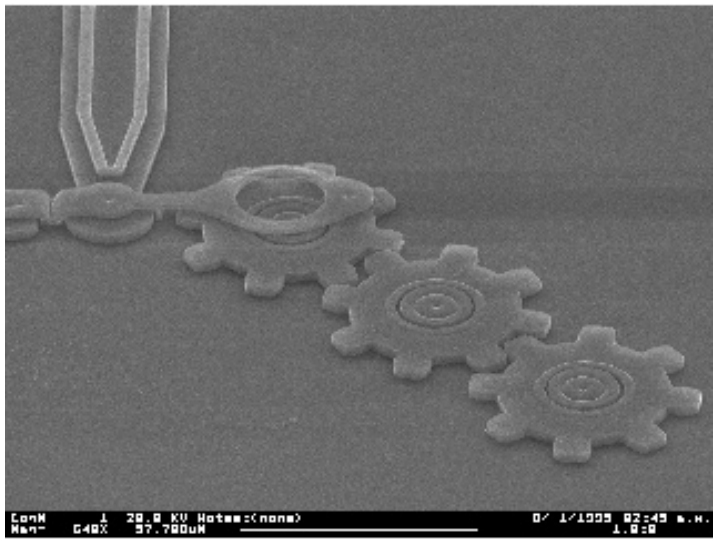
Dimensions of MEMS/NEMS in Perspective



MEMS/NEMS examples shown are of a vertical single-walled carbon nanotube (SWCNT) transistor (5 nm wide and 15 nm high), of molecular dynamic simulations of a carbon-nanotube-based gear, quantum-dot transistor, and digital micromirror device (DMD *http://www.dlp.com*)

Examples of MEMS - gears/motors





- MEMS motor was developped in lates 1980s using polycrystalline silicon (polysilicon) technology
- left-top photo shows micro-gears
  fabricated in mid-1990s using a five-level polysilicon surface micromachining technology (J. J. Sniegowski et al. IEEE Solid-St. Sens. Actuat. Workshop, 178–182 (1996)) -
  one of the most advanced surface micromachining fabrication process developed to date
- left-bottom SEM photo - microengine output gear and two additional driven gears
  gear extreme diameter is approximately 50 micrometers and gear thickness is 2.5 micrometers (J. J. Sniegowski et al.)