7. Introduction to Micro/Nanofabrication

This chapter outlines and discusses important micro- and nanofabrication techniques. We start with the most basic methods borrowed from the integrated circuit (IC) industry, such as thin film deposition, lithography and etching, and then move on to look at MEMS and nanofabrication technologies. We cover a broad range of dimensions, from the micron to the nanometer scale. Although most of the current research is geared towards the nanodomain, a good understanding of top-down methods for fabricating micron-sized objects can aid our understanding of this research. Due to space constraints, we have focused here on the most important technologies; in the microdomain these include surface, bulk and high aspect ratio micromachining; in the nanodomain we concentrate on e-beam lithography, epitaxial growth, template manufacturing and self-assembly. MEMS technology is maturing rapidly, with some new technologies displacing older ones that have proven to be unsuited to manufacture on a commercial scale. However, the jury is still out on methods used in the nanodomain, although it appears that bottom-up methods are the most feasible, and these will have a major impact in a variety of application areas such as biology, medicine, environmental monitoring and nanoelectronics.

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Recent innovations in the area of micro/nanofabrication have created a unique opportunity to manufacture nanometer- to millimeter-sized structures. This wide (six orders of magnitude) range of sizes is applicable to novel electronic, optical, magnetic, mechanical and chemical/biological devices, with applications ranging from sensors to computation and control. In this chapter, we will introduce major micro/nanofabrication techniques currently used to fabricate structures ranging from nanometers to several hundred microns in size. We will mainly focus on the most important and widely used techniques and will not discuss specialized methods. After a brief introduction to basic microfabrication, we will discuss MEMS-fabrication techniques used to build microstructures down to about 1 μm in size. Following this, we will discuss several major top-down and bottom-up nanofabrication methods which have shown great promise in the manufacture of nanostructures (dimensions $< 1\,\mu m$).

7.1 Basic Microfabrication Techniques

Most micro/nanofabrication techniques have their roots in standard fabrication methods developed for the semiconductor industry [7.1–3]. Therefore, a clear understanding of these techniques is needed by anyone embarking on a research and development path in the micro/nano area. In this section, we will discuss

the microfabrication methods most commonly used in the manufacture of micro/nanostructures. Some of these techniques, such as thin-film deposition and etching, are common to the micro/nano and VLSI microchip fabrication disciplines. However, several other techniques that are more specific to the micro/nanofabrication area will also be discussed in this section.

7.1.1 Lithography

Lithography is the technique used to transfer a computer-generated pattern onto a substrate (such as silicon, glass or GaAs). This pattern is then used to etch an underlying thin film (such as an oxide or nitride) for various purposes (including doping and etching). Although photolithography, in other words the lithography using a UV light source, is by far the most common lithography technique in microelectronic fabrication, electron-beam (e-beam) and X-ray lithography are two other alternatives which have attracted considerable attention in the MEMS and nanofabrication areas. We will discuss photolithography in this section and postpone our discussion of e-beam and X-ray techniques to subsequent sections dealing with MEMS and nanofabrication.

The starting point for a specific fabrication sequence (subsequent to the creation of the mask layout on a computer) is the generation of a photomask. This involves a sequence of photographic processes (using optical or e-beam pattern generators) that results in a glass plate that exhibits the desired pattern in the form of a thin ($\approx$ 100 nm) chromium layer. Following the generation of a photomask, the lithography process proceeds as shown in Fig. 7.1. This sequence demonstrates pattern transfer onto a substrate coated with silicon dioxide; however, the same technique is applicable to other materials. After depositing the desired material on the substrate, the process involves spin-coating the substrate with a photoresist. This is a polymeric photosensitive material which can be spun onto the wafer in liquid form (an adhesion promoter such as hexamethyldisilazane, HMDS, is usually used prior to the application of the resist). The spin speed and photoresist viscosity determine the final resist thickness, which is typically between 0.5–2.5 μm. Two different kinds of photoresist are available: positive and negative. In a positive resist, the UV-exposed areas are dissolved in the subsequent development stage, whereas in a negative photoresist, the exposed areas remain intact after development. Due to the better process control that can be achieved for small geometries, the positive resist is most commonly used in VLSI processes. After spinning the photoresist onto the wafer, the substrate is soft-baked (5–30 min at 60–100 °C) in order to remove the solvents from the resist and to improve the adhesion. Subsequently, the mask is aligned to the wafer and the photoresist is exposed to a UV source.

Fig. 7.1 Lithography process flow

Depending on the separation between the mask and the wafer, three different exposure systems are available: 1) contact, 2) proximity, and 3) projection. Although contact printing gives a better resolution than the proximity technique, the constant contact of the mask with the photoresist reduces the process yield and can damage the mask. Projection printing uses a dual-lens optical system to project the mask image onto the wafer. Since only one die can be exposed at a time, this requires a step and repeat system to completely cover the wafer area. Projection printing is far and away the most popular microfabrication system and it can yield superior resolutions to the contact and proximity methods. The exposure source used for photolithography depends on the resolution. Above 0.25 μm minimum line width, a high-pressure mercury lamp is adequate (436 nm g-line and 365 nm i-line). However, between 0.25 and 0.13 μm, deep UV sources such as excimer

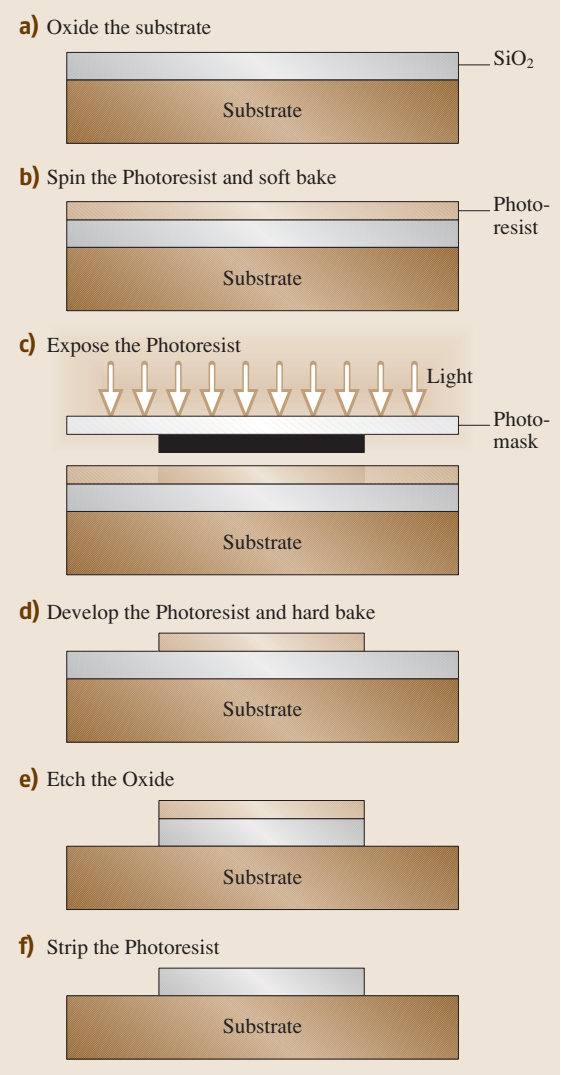


Fig. 7.2 Schematic of photolithography with a positive PR

lasers (248 nm KrF and 193 nm ArF) are required. Although there has been extensive competition between techniques (including e-beam and X-ray) in the below 0.13 μm regime, extreme UV (EUV) (with a wavelength of 10–14 nm) seems to be the preferred technique [7.4].

After exposure, the photoresist is developed in a process similar to the development of photographic films. The resist is subsequently hard baked (20–30 min at 120–180 °C) in order to improve adhesion still further. The hard bake step, which concludes the photolithography process, creates the desired pattern on the wafer. Next, the underlying thin film is etched and the photoresist is stripped in acetone or another organic removal solvent. Figure 7.2 shows a schematic of the steps involved in photolithography with a positive photoresist.

7.1.2 Thin Film Deposition and Doping

Thin film deposition and doping are used extensively in micro/nanofabrication technologies. Most of the fabricated micro/nanostructures contain materials other than that of the substrate, which are obtained by various deposition techniques or by modifying the substrate. The following is a list of a few typical applications for the deposited and/or doped materials used in micro/nanofabrication, which gives an idea of the properties required:

- Mechanical structures
- Electrical isolation
- Electrical connection
- Sensing or actuating
- Mask for etching and doping
- Support or mold during the deposition of other materials (sacrificial materials)
- Passivation

Most of the thin films deposited have different properties to those of their corresponding "bulk" forms (for example, metals shows higher resistivities than a thin film). In addition, the techniques utilized to deposit these materials have a huge impact on their final properties. For instance, the internal stress (compressive or tensile) in

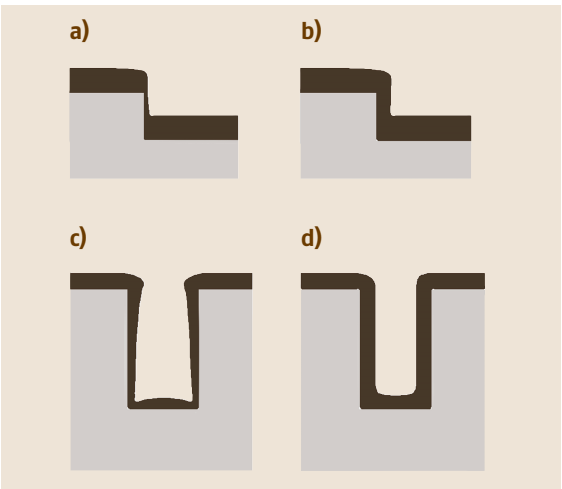


Fig. 7.3a–d Step coverage and conformality: **(a)** poor step coverage, **(b)** good step coverage, **(c)** nonconformal layer, and **(d)** conformal layer.

a film is strongly process-dependent. Excessive stress may crack or detach the film from the substrate and should therefore be minimized, although this property may also be useful for certain applications. Adhesion is another important issue that needs to be taken into account when depositing thin films. In some cases, such as the deposition of noble metals (including gold), an intermediate layer (chromium or titanium) may be needed to improve the adhesion. Finally, step coverage and conformality are two properties that can also influence the choice of one or another deposition technique. Figure 7.3 illustrates these concepts.

Oxidation

Silicon oxidation is a process used to obtain a thin film of SiO_2 with excellent quality (very low density of defects) and thickness homogeneity. Although it is not strictly a deposition, the result is the same: a thin layer of a new material coats the surface. Oxidation is typically performed at temperatures of 900 °C to 1200 °C in the presence of O_2 (dry oxidation) or H_2O (wet oxidation). The reactions for oxide formation are:

$$Si_{(solid)} + O_{2(gas)} \Rightarrow SiO_{2(solid)}$$

and

$$Si_{(solid)} + 2H_2O_{(steam)} \Rightarrow SiO_{2(solid)} + 2H_{2(gas)}$$

Although the rate of oxide growth is higher for wet oxidation, this is achieved at the expense of lower oxide quality (density). Since silicon atoms from the substrate participate in the reaction, the substrate is consumed as the oxide grows ($\approx 44\%$ of the total thickness lies above the line of the original silicon surface). The oxidation of silicon also occurs at room temperature, but a layer of about 20 Å (native oxide) is enough to passivate the surface and prevent further oxidation. To grow thicker oxides, wafers are introduced into an electric resistance furnace such as the one shown in Fig. 7.4, which can process tens of wafers can be processed in a single batch. By strictly controlling the timing, temperature and gas flow entering the quartz tube, the desired thickness can be achieved with a high accuracy. Thicknesses ranging from a few tens of Angstroms to 2 μm can be obtained in a reasonable time. Despite the high quality of the SiO_2 obtained by silicon oxidation (also called *thermal oxide*), the use of this process is often limited to the early stages of fabrication, since some of the materials added during the formation of structure may not stand the high temperatures involved. The furnace can also become contaminated when the substrates have previously been in contact with certain etchants such as KOH, or when materials such as metals have been deposited, also pose limitations in most cases.

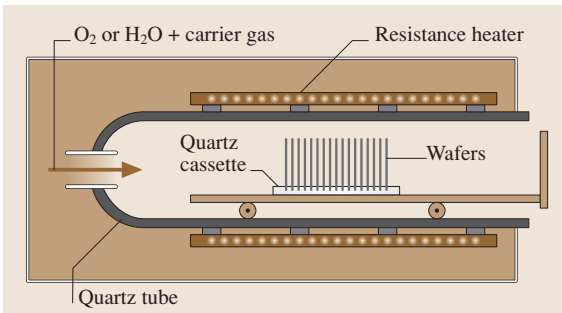


Fig. 7.4 Schematic of a typical oxidation furnace

Doping

The introduction of certain impurities into a semiconductor can change its electrical, chemical, and even mechanical properties. Typical impurities or *dopants* used in silicon include boron (to form p-type regions) and phosphorus or arsenic (to form n-type regions). Doping is the main process used to fabricate major components such us diodes and transistors in the microelectronic industry. In micro/nanofabrication technologies, doping has additional applications, such as the formation of piezoresistors for mechanical transducers or the creation of etch stop layers. Two different techniques are used to introduce the impurities into a semiconductor substrate: diffusion and ion implantation.

Diffusion, a process used to form n- and p-type regions in silicon, dominated integrated circuit manufacture in the period just after such circuits had been invented. The diffusion of impurities into the silicon only occurs at high temperatures (above 800 °C). The furnaces used to carry out this process are similar to the ones used for oxidation. The dopants are introduced into the gaseous atmosphere of the furnace from liquid or solid sources. Figure 7.5 illustrates the process of creating an n-type region by the diffusion of phosphor from the surface into a p-type substrate. A masking material must have been previously deposited and patterned on the surface in order to define the areas to be doped. However, because diffusion is an isotropic process, the doped area will also extend underneath the mask. In microfabrication, diffusion is mainly used in the formation of very highly doped boron regions (p^{++}), which are usually used as etch stops in bulk micromachining.

Ion implantation allows more precise control of the dose (total amount of impurities introduced per area unit) and the impurity profile (concentration versus depth). In ion implantation, the impurities are ionized and accelerated towards the semiconductor surface. The penetration of impurities into the material follows a Gaussian distribution. After implantation, an annealing process is needed to activate the impurities and to repair the damage in the crystal structure produced by the ion collisions. A *drive-in* process to redistribute the impurities, performed in a standard furnace like those used for oxidation or diffusion may also be required.

Chemical Vapor Deposition and Epitaxy

As its name suggests, chemical vapor deposition (CVD) includes all of the deposition techniques that make use of chemical reactions in the gas phase to form the deposited thin film. The energy needed for the chemical reaction to occur is usually supplied by maintaining the substrate at elevated temperatures. Alternative energy sources, such as plasma or optical excitation, are also used because they enable a lower substrate temperature. The most common CVD processes in microfabrication are LPCVD (low pressure CVD) and PECVD (plasma-enhanced CVD).

The LPCVD process is typically carried out in electrically heated tubes, similar to oxidation tubes, equipped with pumps needed to achieve the low pressures (0.1 to 1.0 torr) required. Large numbers of wafers can be processed simultaneously and the material is deposited on both sides of the wafers. The process temperatures depend on the material to be deposited, but are generally in the range of 550 to 900 °C. As in the oxidation, high temperatures and contamination issues can restrict the type of processes used before LPCVD. Typical materials deposited by LPCVD include silicon oxide (for example $SiCl_2H_2 + 2N_2O \Rightarrow SiO_2 + 2N_2 + 2HCL$ at 900 °C), silicon nitride (such as $3SiH_4 + 4NH_3 \Rightarrow Si_3N_4 + 12H_2$, at 700–900 °C), and polysilicon (for instance $SiH_4 \Rightarrow Si + 2H_2$ at 600 °C). Due to its faster etch rate in HF, in situ phosphorus-doped LPCVD oxide (phosphosilicate glass or PSG) is used extensively in surface micromachining as the sacrificial layer. The conformality in this process is excellent, even for structures with very high aspect ratios. The mechanical properties of LPCVD materials are good compared to others such as PECVD, and are often used as structural materials in microfabricated devices. The stress in the deposited layers depends on the material, deposition conditions, and subsequent thermal history (for example the post-deposition anneal). Typical values are: 100–300 MPa (compressive) for oxide, ≈ 1 GPa (tensile) for stoichiometric nitride, and ≈ 200–300 MPa (tensile) for polysilicon. The stress present in the nitride layers can be reduced to almost zero using a silicon-rich composition. Since the stress values can vary over a wide range, it is important to measure and characterize the internal stress of deposited thin films for any particular set of equipment and deposition conditions.

The PECVD process is performed in plasma systems such as the one represented in Fig. 7.6. The use of RF energy to create highly reactive species in the plasma allows lower temperatures to be used at the substrate (150 to 350 °C). The parallel-plate plasma reactors normally used in microfabrication can only process a limited number of wafers per batch. The wafers are positioned horizontally on top of the lower electrode so that only one side gets deposited. Typical materials deposited with PECVD include silicon oxide, nitride, and amorphous silicon. Conformality

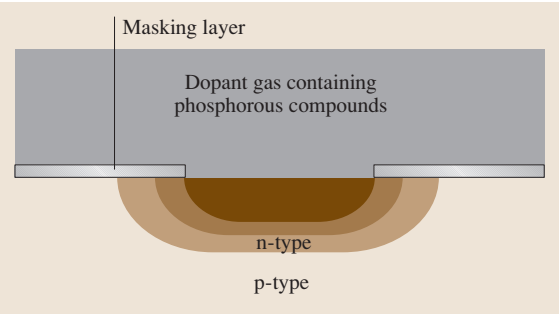


Fig. 7.5 Formation of an n-type region on a p-type silicon substrate by diffusion of phosphorus

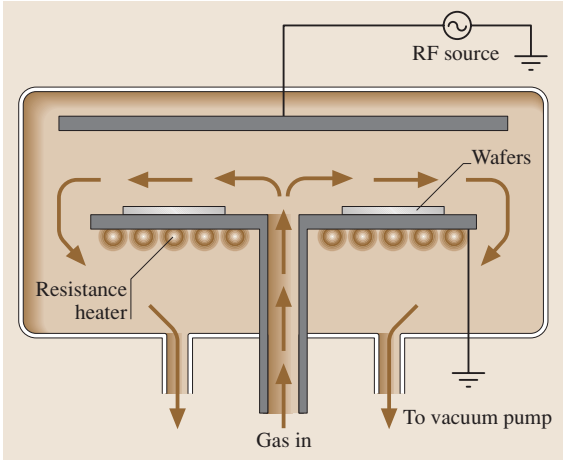


Fig. 7.6 Schematic of a typical PECVD system

is good for structures with low aspect ratios, but becomes very poor for deep trenches (20% of the surface thickness inside through-wafer holes with an aspect ratio of 10). The stress depends on deposition parameters and can be either compressive or tensile. PECVD nitrides are typically nonstoichiometric (Si_xN_y) and are much less resistant to etchants in masking applications.

Another interesting type of CVD is epitaxial growth. In this process, a single-crystalline material is grown as an extension of the crystal structure of the substrate. It is possible to grow dissimilar materials if the crystal structures are somehow similar (lattice-matched). Silicon-on-sapphire (SOS) substrates and some heterostructures are fabricated in this way. However, deposition of silicon on another silicon substrate is the most common CVD technique. Selective epitaxial growth is of particular interest for the formation of microstructures. In this process, the silicon crystal is only allowed to grow in windows patterned on a masking material. Many CVD techniques have been used to produce epitaxial growth. The most common method used for silicon is thermal chemical vapor deposition or vapor-phase epitaxy (VPE). Metallorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) commonly used to grow high-quality III–V compound layers with nearly atomic abrupt interfaces. The former uses vapors of organic compounds with group III atoms such as trimethylgallium [$Ga(CH_3)_3$] and group V hydrides such as AsH_3 in a CVD chamber with fast gas switching capabilities. The latter typically uses molecular beams from thermally evaporated elemental sources aimed at the substrate in an ultrahigh vacuum chamber. In this case, rapid on/off control of the beams is achieved by employing shutters in front of the source. Finally, it should be mentioned that many metals (molybdenum, tantalum, titanium and tungsten) can also be deposited using LPCVD. These are attractive due to their low resistivities and their ability to form silicides with silicon. Due to its application in new interconnect technologies, copper CVD is an active area of research.

Physical Vapor Deposition (Evaporation and Sputtering)

In physical deposition systems, the material to be deposited is transported from a source to the wafers, both of which are in the same chamber. Two physical principles are used to achieve this: evaporation and sputtering.

In evaporation, the source is placed in a small container with tapered walls, called a crucible, and is heated up to a temperature where evaporation occurs. Various techniques are utilized to reach the high temperatures needed, including the induction of high currents with coils wound around the crucible and the bombardment of the material surface with an electron beam (e-beam evaporators). This process is mainly used to deposit metals, although dielectrics can also be evaporated. In a typical system the crucible is located at the bottom of a vacuum chamber, whereas the wafers line the dome-shaped ceiling of the chamber, Fig. 7.7. The main characteristic of this process is very poor step coverage, including shadow effects, as illustrated in Fig. 7.8. As explained in subsequent sections, some microfabrication techniques utilize these effects to pattern the deposited layer. One way to improve the step coverage is to rotate and/or heat the wafers during the deposition.

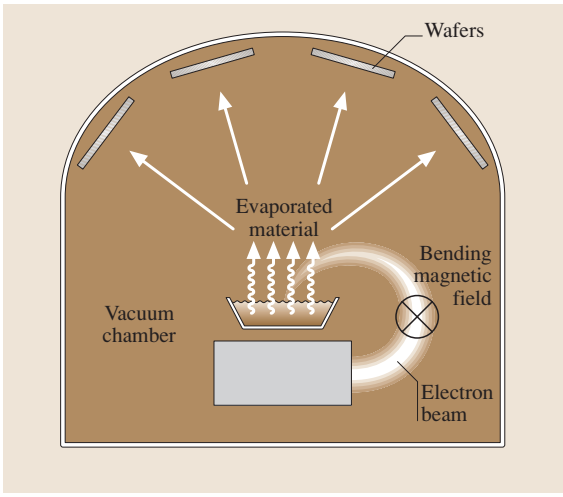


Fig. 7.7 Schematic of an e-beam deposition system

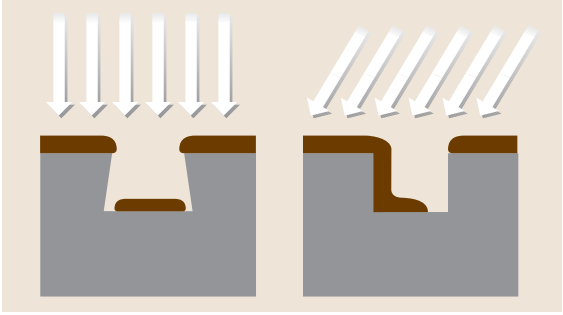


Fig. 7.8 Shadow effects observed in evaporated films. *Arrows* show the trajectory of the material atoms being deposited

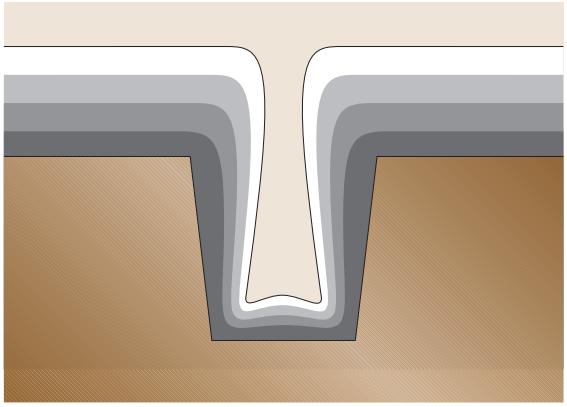


Fig. 7.9 Typical cross-section evolution of a trench being filled via sputter deposition

During sputtering, a target of the material to be deposited is bombarded with high-energy inert ions (usually argon). The outcome of the bombardment is that individual atoms or clusters are removed from the surface and ejected towards the wafer. The physical nature of this process permits its use with virtually any existing material. Examples of interesting materials for microfabrication that are frequently sputtered include metals, dielectrics, alloys (such as shape memory alloys), and all kinds of compounds (for example piezoelectric PZT). The inert ions used to bombard the target are produced in DC or RF plasma. In a simple parallel-plate system the top electrode is the target and the wafers are placed horizontally on top of the bottom electrode. Despite its lower deposition rate, the step coverage achieved via sputtering is much better than that gained from evaporation. However, the films obtained with this deposition process are nonconformal. Figure 7.9 illustrates successive sputtering profiles in a trench.

Both evaporation and sputtering systems are often capable of depositing more than one material simultaneously or sequentially. This ability is very useful for obtaining alloys and multilayers (for instance, multilayer magnetic recording heads are sputtered). For certain low-reactivity metals such as Au and Pt, the previous deposition of a thin layer of another metal is needed to improve the adhesion. Ti and Cr are two adhesion promoters frequently used. The stress in evaporated or sputtered layers is typically tensile. The deposition rates are much higher than most CVD techniques. However, due to stress accumulation and cracking, a thickness of more than 2 μm is rarely achieved with these processes. The technique described in the next section is sometimes used for thicker depositions.

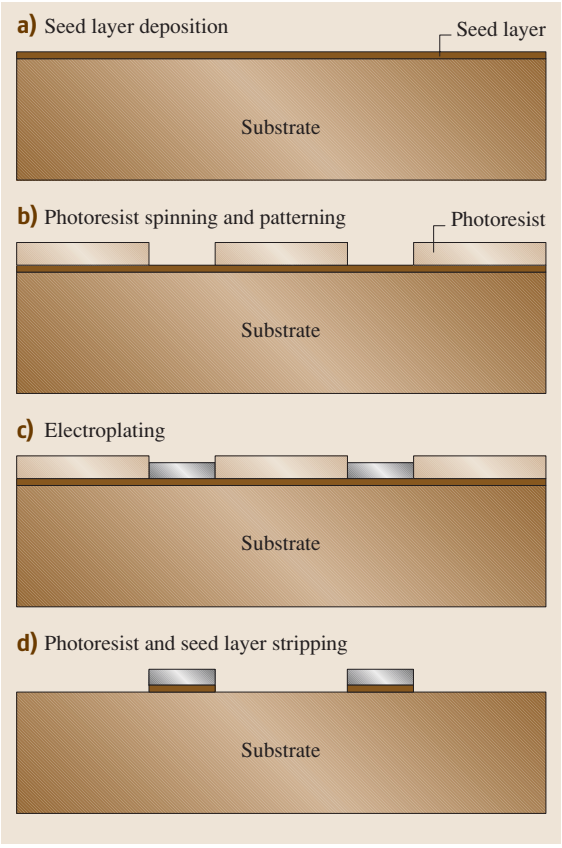


Fig. 7.10a–d Formation of isolated metal structures by electroplating through a mask: **(a)** seed layer deposition, **(b)** photoresist spinning and patterning, **(c)** electroplating, **(d)** photoresist and seed layer stripping

Electroplating

Electroplating (or electrodeposition) is a process typically used to obtain thick (tens of μm) metal structures. The sample to be electroplated is placed into a solution containing a reducible form of the ion of the desired metal, and it is maintained at a negative potential (cathode) relative to a counter electrode (anode). The ions are reduced at the sample surface and the nonsoluble metal atoms are incorporated into the surface. As an example, copper electrodeposition is frequently performed in copper sulfide-based solutions. The reaction that takes place at the surface is $Cu^{2+} + 2e^- \rightarrow Cu_{(s)}$. Recommended current densities for electrodeposition processes are on the order of 5 to 100 mA/cm^2.

As can be deduced from the process mechanism, the surface to be electroplated must be electrically conductive, and preferably of the same material as the deposited

one if a good adhesion is desired. In order to electrodeposit metals on top of an insulator (the most frequent case) a thin film of the same metal, called the seed layer, is deposited on the surface first. Masking the seed layer with a resist permits selective electroplating at the patterned areas. Figure 7.10 illustrates the sequence of steps typically required to obtain isolated metal structures.

Pulsed Laser and Atomic Layer Deposition

Pulsed laser and atomic layer deposition techniques have attracted a considerable amount of attention recently. These two techniques offer several unique advantages compared to other thin film deposition methods that are particularly useful for next-generation nanoscale device fabrication. Pulsed laser deposition (PLD) is a simple technique that uses an intense (1 GW within 25 ns) UV laser (such as KrF excimer) to ablate a target material [7.5]. Plasma is subsequently formed from the target and is deposited on the substrate. Multitarget systems with Auger and RHEED spectroscopes are commercially available. Figure 7.11 shows a typical PLD deposition set-up. The main advantages of the PLD are its simplicity and ability to deposit complex materials with preserved stoichiometry ("stoichiometry transfer"). In addition, fine control over the film thickness can also be achieved by controlling the number of pulses. Stoichiometry transfer allows many complex targets, such as ferroelectrics, superconductors and magnetostrictives to be deposited using PLD. Other materials deposited include oxides, carbides, polymers, and metallic systems (such as FeNdB).

Atomic layer deposition (ALD) is a gas-phase self-limiting deposition method capable of depositing atomic layer thin films with excellent large area uniformity and conformality [7.6]. It enables simple and accurate control over film composition and thickness at the atomic layer level (typical growth rates of a few Å/cycle). Although recent research has focused upon depositing high-k dielectric materials (Al_2O_3, and HfO_2) for next-generation CMOS electronics, other materials can also be deposited. These include transition metals (Cu, Co, Fe, and Ni), metal oxides, sulfides, nitrides and fluorides. Atomic-level control over film thickness and composition are also attractive features for MEMs application, such as conformal 3D packaging and air-gap structures. ALD is a modification of the CVD process and is based on two or more vapor-phase reactants that are introduced into the deposition chamber in a sequential manner. One growth cycle consists of four steps. First, a precursor vapor is introduced into the chamber, resulting in the deposition of a self-limiting monolayer on the surface of the substrate. Then the extra unreacted vapor is pumped out and a vapor dose of a second reactant is introduced. This reacts with the precursor on the surface in a self-limiting fashion. Finally, the extra unreacted vapor is pumped out and the cycle is repeated.

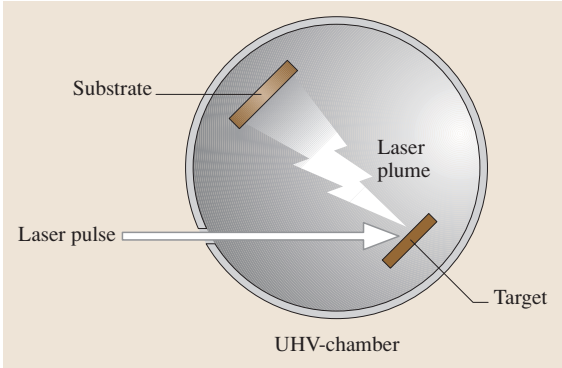


Fig. 7.11 A typical PLD deposition set-up

7.1.3 Etching and Substrate Removal

Thin film and bulk substrate etching is another fabrication step that is of fundamental importance to both VLSI processes and micro/nanofabrication. In the VLSI area, various conducting and dielectric thin films deposited for passivation or masking purposes need to be removed at some point. In micro/nanofabrication, in addition to thin film etching, the substrate (silicon, glass, GaAs) usually also needs to be removed in order to create various me-

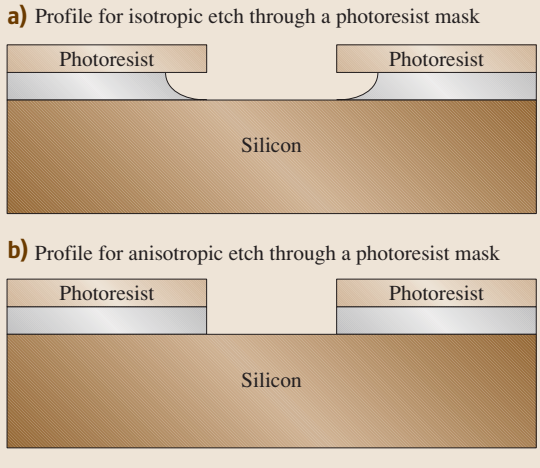


Fig. 7.12a,b Profile for isotropic (**a**) and anisotropic (**b**) etch through a photoresist mask

chanical micro/nanostructures (beams, plates and so on). Two important figures of merit for any etching process are selectivity and directionality. Selectivity is the degree to which the etchant can differentiate between the masking layer and the layer to be etched. Directionality relates to the etch profile under the mask. In an isotropic etch, the etchant attacks the material in all directions at the same rate, hence creating a semicircular profile under the mask, Fig. 7.12a. In an anisotropic etch, the dissolution rate depends on the specific direction and one can obtain straight sidewalls or other noncircular profiles, Fig. 7.12b. One can also divide the various etching techniques into wet and dry categories. We will use this classification in this section, discussing different wet etchants first and then the dry etching techniques used most often in the micro/nanofabrication.

Wet Etching

Historically, wet etching techniques preceded dry techniques. These still constitute an important group of etchants for micro/nanofabrication despite the fact that they are used less frequently in VLSI processes. Wet etchants are, by and large, isotropic, and they show superior selectivity for the masking layer over various dry techniques. In addition, due to the lateral undercut, the minimum feature achievable with wet etchants is limited to $> 3\ \mu m$. Silicon dioxide is commonly etched in a dilute (6:1, 10:1, or 20:1 by volume) or buffered HF (BHF, HF+NH_4F) solution (etch rate of $\approx 1000\ Å/min$ in BHF). Photoresist and silicon nitride are the two most common masking materials used for the wet oxide etch. The wet etchant used for silicon nitride is hot (140–200 °C) phosphoric acid with silicon oxide used as the masking material. Nitride wet etch is not very common (except for blanket etch) due to the masking difficulties and nonrepeatable etch rates. Metals can be etched using various combinations of acids and base solutions. There are also many commercially available etchant formulations for aluminium, chromium and gold which can be easily used. A comprehensive table of various metal etchants can be found in [7.7].

Anisotropic and isotropic wet etching of crystalline (silicon and gallium arsenide) and noncrystalline (glass) substrates is an important topic in micro/nanofabrication [7.8–11]. In particular, the achievement of anisotropic wet etching of silicon is considered to mark the beginning of the micromachining and MEMS field. Isotropic etching of silicon using $HF/HNO_3/CH_3COOH$ (various different formulations have been used) dates back to the 1950s and is still frequently used to thin down the silicon wafer. The etch mechanism for this combination has been elucidated and is as follows: HNO_3 is used to oxidize the silicon which is subsequently dissolved away in the HF. The acetic acid is used to prevent the dissociation of HNO_3 (the etch works as well without the acetic acid). For short etch times, silicon dioxide can be used as the masking material; however, one needs to use silicon nitride if a longer etch time is desired. This etch also shows dopant selectivity, with the etch rate dropping at lower doping concentrations ($<10^{17}\ cm^{-3}$ n- or p-type). Although this effect can potentially be used as an etch stop mechanism in order to fabricate microstructures, the masking problem has prevented widespread application of this approach. Glass can also be isotropically etched using the HF/HNO_3 combination, with the etch surfaces showing considerable roughness. This has been extensively used for fabricating microfluidic components (mainly channels). Although Cr/Au is usually used as the masking layer, long etch times require a more robust mask (bonded silicon has been used for this purpose).

Silicon anisotropic wet etch constitutes an important technique in bulk micromachining. The three most important silicon etchants in this category are potassium hydroxide (KOH), ethylene diamine pyrocatechol (EDP) and tetramethyl ammonium hydroxide (TMAH). These are all anisotropic etchants which attack silicon along preferred crystallographic directions. In addition, they all show a marked reduction in the etch rate in heavily doped ($> 5\times10^{19}\ cm^{-3}$) boron ($p^{++}$) regions. The chemistry behind the action of these etchants is not yet very clear, but it seems that silicon atom oxidation at the surface and the reaction of silicon with hydroxyl ions (OH^-) are responsible for the formation of a soluble silicon complex ($SiO_2(OH)^{2-}$). The etch rate depends on the concentration and temperature and is usually around $1\ \mu m/min$ at temperatures of 85–115 °C. Common masking materials for anisotropic wet etchants are silicon dioxide and nitride, with the latter being superior for longer etch times. The crystallographic plane which shows the slowest etch rate is the (111) plane. Although it has been speculated that the lower atomic concentration along these planes is the reason for this phenomenon, the evidence is inconclusive and other factors must be included to account for this remarkable etch stop property. The anisotropic behavior of these etchants with respect to the (111) plane has been used extensively to create beams, membranes and other mechanical and structural components. Figure 7.13 shows typical cross-sections of (100) and (110) silicon wafers etched with an anisotropic wet etchant. As can be seen, the (111) slow

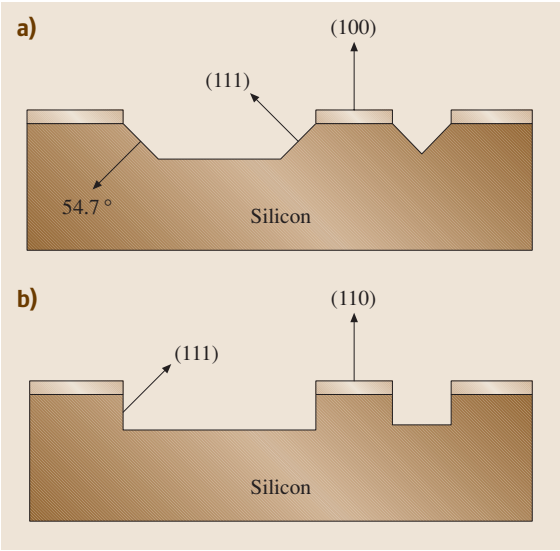


Fig. 7.13a,b Anisotropic etch profiles for: **(a)** (100), and **(b)** (110) silicon wafers

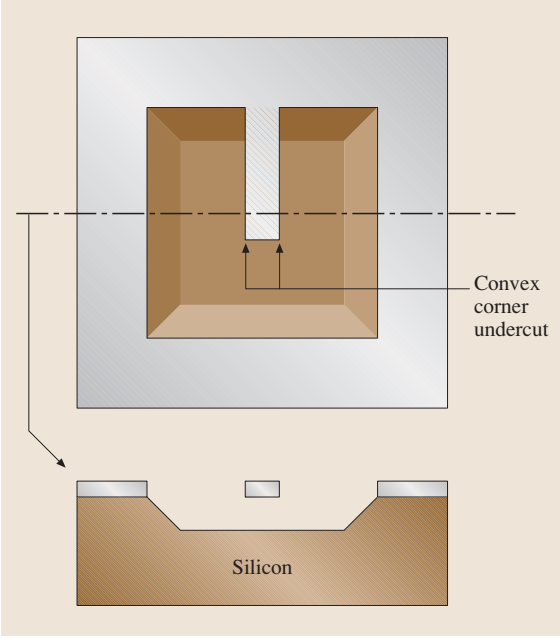


Fig. 7.14 Top view and cross-section of a dielectric cantilever beam fabricated using convex corner undercutting

planes are exposed in both situations, one creating 54.7° sloped sidewalls in the (100) wafer and the other creating vertical sidewalls in the (110) wafer. Depending on the dimensions of the mask opening, a V-groove or a trapezoidal trench is formed in the (100) wafer. A large enough opening will allow the silicon to be etched all the way through the wafer, thus creating a thin dielectric membrane on the other side. It should be mentioned that the exposed convex corners have a higher etch rate than the concave ones, resulting in an undercut which can be used to create dielectric (such as nitride) cantilever beams. Figure 7.14 shows a cantilever beam fabricated using the convex corner undercut on a (100) wafer.

The three above-mentioned etchants show different directional and dopant selectivities. KOH has the best (111) selectivity (400/1), followed by TMAH and EDP. However, EDP has the highest selectivity with respect to the deep boron diffusion regions. Safety and CMOS compatibility are other important criteria for choosing a particular anisotropic etchant. Among the three mentioned etchants, TMAH is the most benign one, whereas EDP is extremely corrosive and carcinogenic. Silicon can be dissolved in TMAH in order to improve its selectivity with respect to aluminium. This property has made TMAH very appealing for post-CMOS micromachining where aluminium lines have to be protected. Finally, it should be mentioned that one can modulate the etch rate using a reversed biased p-n junction (electrochemical etch stop). Figure 7.15 shows the set-up commonly used to perform electrochemical etching. The silicon wafer under etch consists of an n-epi region on a p-type substrate. Upon the application of a reverse bias voltage to the structure (p substrate is in contact with the solution and n-epi is protected using a watertight fixture), the p substrate is etched away. When the n-epi regions are exposed to the solution an oxide passivation layer is formed and the etch is stopped. This technique can be

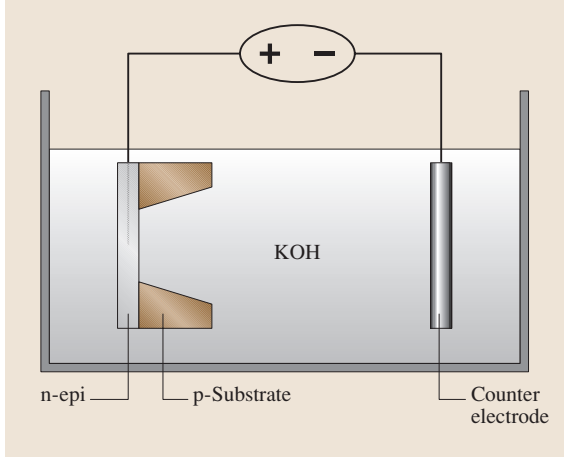


Fig. 7.15 Electrochemical etch set-up

used to fabricate single-crystalline silicon membranes for pressure sensors and other mechanical transducers.

Dry Etching

Most dry etching techniques are plasma-based. They have several advantages when compared with wet etching. These include a smaller undercut (allowing smaller lines to be patterned) and higher anisotropicity (allowing vertical structures with high aspect ratios). However, the selectivities of dry etching techniques are lower than those of wet etchant techniques, and one must take into account the finite etch rate of the masking materials. The three basic dry etching techniques, namely high-pressure plasma etching, reactive ion etching (RIE) and ion milling, utilize different mechanisms to obtain directionality.

Ion milling is a purely physical process which utilizes accelerated inert ions (such as Ar^+) that strike perpendicular to the surface, removing material (pressure $\approx 10^{-4}$–10^{-3} Torr), Fig. 7.16a. The main characteristics of this technique are very low etch rates (on the order of a few nm/min) and poor selectivity (close to 1:1 for most materials); hence it is generally used to etch very thin layers. In high-pressure (10^{-1}–5 Torr) plasma etchers, highly reactive species are created that react with the material to be etched. The products of the reaction are volatile so they diffuse away and new material is exposed to the reactive species. Directionality can be achieved, if desired, with the sidewall passivation technique (Fig. 7.16b). In this technique, nonvolatile species produced in the chamber deposit and passivate the surfaces. The deposit can only be removed by physical collision with incident ions. Because the movement of the ions has a vertical directionality, the deposit is mainly removed at horizontal surfaces, while vertical walls remain passivated. In this fashion, the vertical etch rate becomes much higher than the lateral one.

RIE etching, also called ion-assisted etching, is a combination of physical and chemical processes. In this technique the reactive species react with the material only when the surfaces are "activated" by the collision of incident ions from the plasma (by breaking bonds

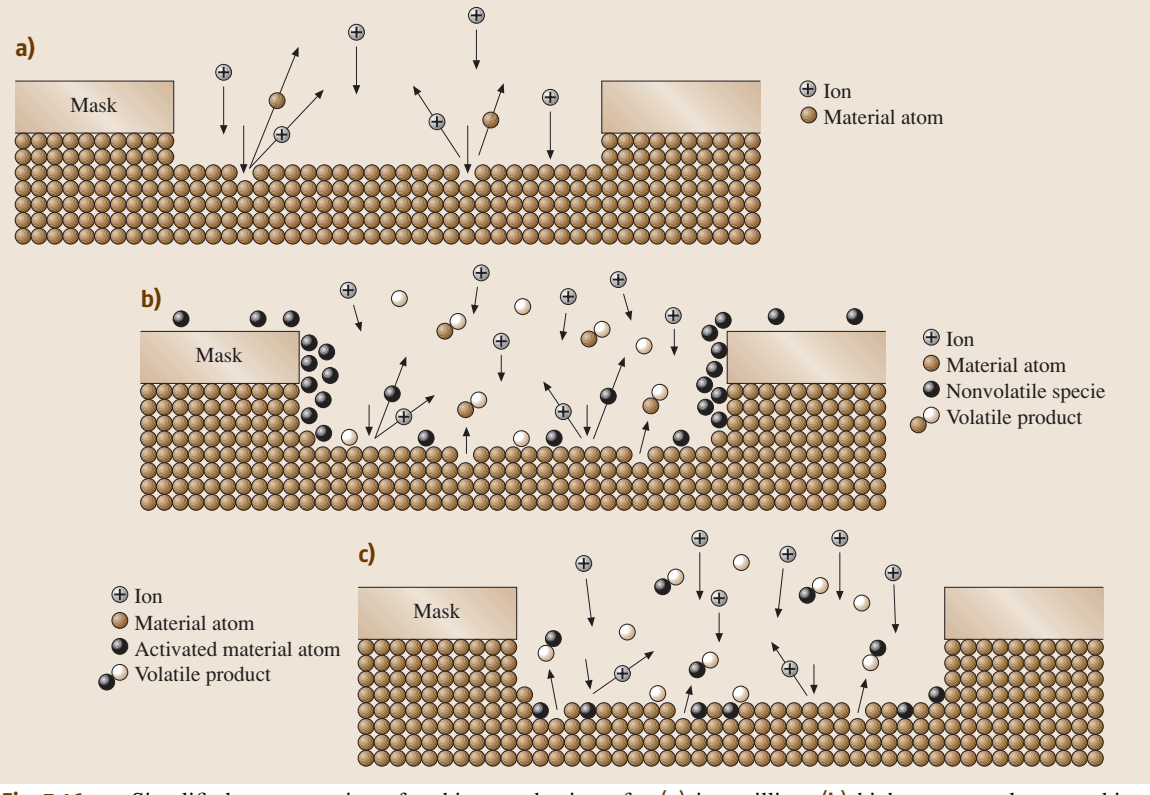


Fig. 7.16a–c Simplified representation of etching mechanisms for **(a)** ion milling, **(b)** high-pressure plasma etching, **(c)** RIE

Table 7.1 Typical dry etch chemistries

Si	CF_4/O_2, CF_2Cl_2, CF_3Cl, $SF_6/O_2/Cl_2$, $Cl_2/H_2/C_2F_6/CCl_4$, C_2ClF_5/O_2, Br_2, SiF_4/O_2, NF_3, ClF_3, CCl_4, CCl_3F_5, C_2ClF_5/SF_6, C_2F_6/CF_3Cl, CF_3Cl/Br_2
SiO2	CF_4/H_2, C_2F_6, C_3F_8, CHF_3/O_2
Si3N4	$CF_4/O_2/H_2$, C_2F_6, C_3F_8, CHF_3
Organics	O_2, CF_4/O_2, SF_6/O_2
Al	BCl_3, BCl_3/Cl_2, $CCl_4/Cl_2/BCl_3$, $SiCl_4/Cl_2$
Silicides	CF_4/O_2, NF_3, SF_6/Cl_2, CF_4/Cl_2
Refractories	CF_4/O_2, NF_3/H_2, SF_6/O_2
GaAs	BCl_3/Ar, $Cl_2/O_2/H_2$, $CCl_2F_2/O_2/Ar/He$, H_2, CH_4/H_2, $CClH_3/H_2$
InP	CH_4/H_2, C_2H_6/H_2, Cl_2/Ar
Au	$C_2Cl_2F_4$, Cl_2, $CClF_3$

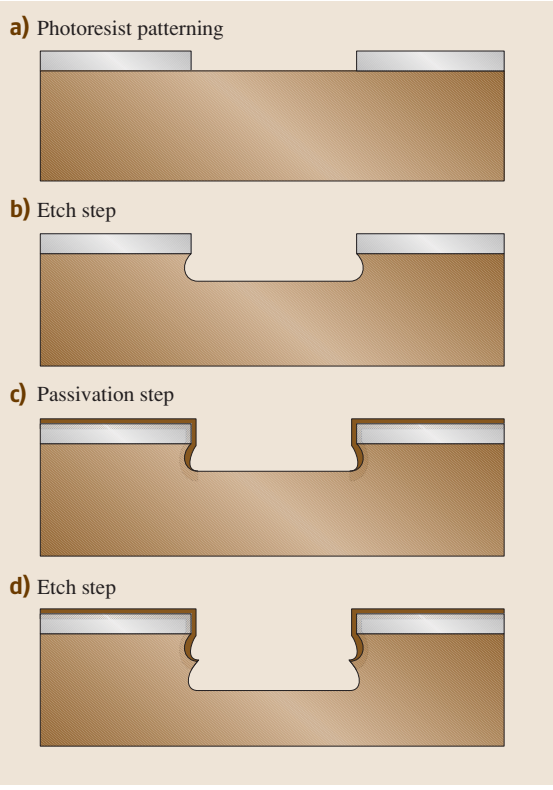


Fig. 7.17a–d DRIE cyclic process: (**a**) photoresist patterning, (**b**) etch step, (**c**) passivation step, (**d**) etch step

at the surface for example). As in the previous technique, the directionality of the ion velocity produces many more collisions in the horizontal surfaces than in the walls, thus generating faster etching rates in the vertical direction (Fig. 7.16c). To further increase the etch anisotropy, sidewall passivation methods are also used in some cases. An interesting case is the deep reactive ion etching (DRIE) technique, capable of achieving aspect ratios of 30:1 and silicon etching rates of 2 to 3 μm/min (through-wafer etch is possible). In this technique, the passivation deposition and etching steps are performed sequentially in a two-step cycle, as shown in Fig. 7.17. In commercial silicon DRIE etchers, SF_6/Ar is typically used for the etching step and a combination of Ar and a fluoropolymer (nCF_2) for the passivation step. A Teflon-like polymer that is only about 50 nm thick is deposited during the latter step, covering only the sidewalls (Ar^+ ion bombardment removes the Teflon on the horizontal surfaces). Due to the cyclic nature of this process, the sidewalls of the etched features show a periodic "wave-shape" roughness of 50 to 400 nm.

Dry etching can also be performed in nonplasma equipment if the etching gases are reactive enough. These "vapor-phase etching" (VPE) processes can be carried out in a simple chamber with gas feeding and pumping capabilities. Two examples of VPE are xenon difluoride (XeF_2) etching of silicon and HF vapor etching of silicon dioxide. Due to their isotropic natures, these processes are typically used for etching sacrificial layers and releasing structures whilst avoiding stiction problems (see sections 7.2.1 and 7.2.2).

A wide range of important materials can be etched using the above-mentioned techniques, and a selection of chemical approaches are available for each material. Table 7.1 lists some of the most common materials along with selected etch recipes [7.12]. For each approach, the etch rate, directionality and selectivity with respect to the mask materials depend on parameters such as the flow rates of the gases entering the chamber, the working pressure and the RF power applied to the plasma.

7.1.4 Substrate Bonding

Substrate (wafer) bonding (silicon–silicon, silicon–glass, and glass–glass) is one of the most important microsystem fabrication techniques [7.13, 14]. It is frequently used to fabricate complex 3-D structures, both as a functional unit and as a part of the final microsystem package and encapsulation. The two most important bonding techniques are silicon–silicon fusion (or silicon direct bonding) and silicon–glass electrostatic (or anodic) bonding. In addition to these techniques, several other alternative methods which utilize an intermediate layer (eutectic, adhesive, and glass frit) have also been investigated. All of these techniques can be used to bond substrates at the wafer level. In this section we will only discuss wafer-level techniques; device-level bonding methods (such as e-beam and laser welding) will not be discussed.

Silicon Direct Bonding

Direct silicon or fusion bonding is used in the fabrication of micromechanical devices and silicon-on-insulator (SOI) substrates. Although it is mostly used to bond two silicon wafers with or without an oxide layer, it has also been used to bond different semiconductors such as GaAs and InP [7.14]. One main requirement for a successful bond is sufficient planarity (<10 Å surface roughness and $< 5\,\mu m$ bow across a 4" wafer) and surface cleanliness. Thermal expansion mismatch also needs to be considered if two dissimilar materials are to be bonded. The bonding procedure is as follows: the silicon- or oxide-coated silicon wafers are first thoroughly cleaned. Then the surfaces are hydrated (activated) in HF or boiling nitric acid (an RCA clean also works). This creates an abundance of hydroxyl ions, rendering the surfaces hydrophilic. Then the substrates are brought into close proximity (starting from the center to avoid void formation). The closeness of the bonding surfaces allows short-range attractive van der Waals forces to bring the surfaces into intimate contact on an atomic scale. Following this step, hydrogen bonds between the two hydroxyl-coated silicon wafers bind the substrates together. These steps can be performed at room temperature; however, in order to increase the bond strength, a high-temperature (800–1200 °C) anneal is usually required. A big advantage of silicon fusion bonding is that the substrates are thermally matched.

Anodic Bonding

Silicon-glass anodic (electrostatic) bonding is another major substrate joining technique which has been extensively used for microsensor packaging and device fabrication. The main advantage of this technique is its lower bonding temperature, which is around 300–400 °C. Figure 7.18 shows the bonding set-up. A glass wafer (Pyrex 7740 is often used due to its good thermal expansion match to silicon) is placed on top of a silicon wafer and the sandwich is heated to 300–400 °C. Subsequently, a voltage of ≈ 1000 V is applied to the glass–silicon sandwich with the glass connected to the cathode. The bond starts immediately after the application of the voltage and spreads outward from the cathode contact point. The bond can be visually observed as a dark grayish front which expands throughout the wafer.

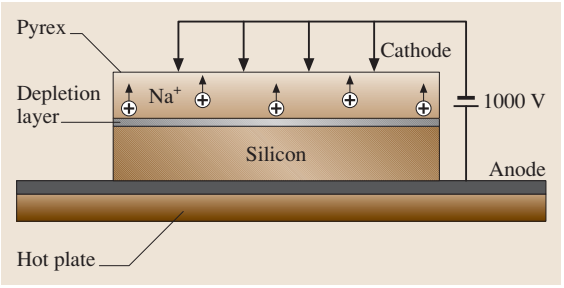


Fig. 7.18 Set-up for anodic bonding of glass to silicon

The bonding mechanism is as follows. During the heating period, glass sodium ions move toward the cathode and create a depletion layer at the silicon–glass interface. A strong electrostatic force is therefore created at the interface which pulls the substrates into an intimate contact. The exact chemical reaction responsible for anodic bonding is not yet clear but covalent silicon–oxygen bonds at the interface seems to be responsible for the bond. Silicon-to-silicon anodic bonding using sputtered or evaporated glass interlayers is also possible.

Bonding with Intermediate Layers

Various other wafer bonding techniques utilizing an intermediate layer have also been investigated [7.14]. Among the most important ones are adhesive, eutectic, and glass frit bonds. Adhesive bonds, achieved by inserting a polymer (polyimides, epoxies, thermoplast adhesives, and photoresists) between the wafers, have been used to join different wafer substrates [7.15]. Complete curing (in the oven or using dielectric heating) of the polymer before or during the bonding process prevents subsequent solvent outgas and void formation. Although reasonably high bonding strengths can be obtained, these bonds are nonhermetic and unstable over reasonably long periods of time.

In the eutectic bonding process, gold-coated silicon wafers are bonded together at temperatures greater than the silicon–gold eutectic point (363 °C, 2.85% silicon and 97.1% Au) [7.16]. This process can achieve high bonding strength and good stability at relatively low temperatures. For good bond uniformity, silicon dioxide must be removed from the silicon surface prior to the deposition of the gold. In addition, all organic contaminants must be removed from the surface of the gold (using UV light) prior to bonding. Pressure must also be applied in order to achieve a better contact. Although eutectic bonds can be achieved at low temperatures, attaining uniformity over large areas has proven to be a challenging task.

Glass frit can also be used as an interlayer in substrate bonding. In this technique, a thin layer of glass is first deposited and preglazed. The glass-coated substrates are then brought into contact and the sandwich is heated to above the glass melting temperature (typically $< 600\,°C$). As for the eutectic process, pressure must be applied for an adequate contact to occur [7.17].

7.2 MEMS Fabrication Techniques

In this section, we will discuss various MEMS fabrication techniques commonly used to build various microdevices (microsensors and microactuators) [7.8–11]. The size range of the microstructures that can be fabricated using these techniques spans from 1 mm to 1 μm. As was mentioned in the *Introduction*, we will concentrate on the more important techniques, skimming over specialized methods.

7.2.1 Bulk Micromachining

Bulk micromachining is the oldest MEMS technology and therefore one of the most mature [7.18]. It is currently the most commercially successful MEMS technique by some distance, and is used to manufacture devices such as pressure sensors and ink-jet print heads. Although there are many different variations, the basic concept behind bulk micromachining is selective removal of the substrate (silicon, glass, GaAs, and so on). This allows the creation of various micromechanical components such as beams, plates and membranes which can be used to fabricate a variety of sensors and actuators. The most important microfabrication techniques used in bulk micromachining are wet and dry etch and substrate bonding. Although one can use different criteria to divide bulk micromachining techniques into separate categories, we will use a historical timeline for this purpose. We will start by discussing the more traditional wet etching techniques, and then proceed to discuss the more recent ones using deep RIE and wafer bonding.

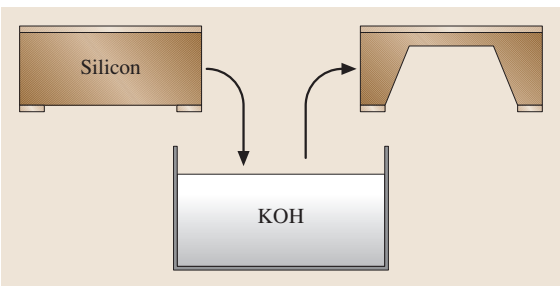
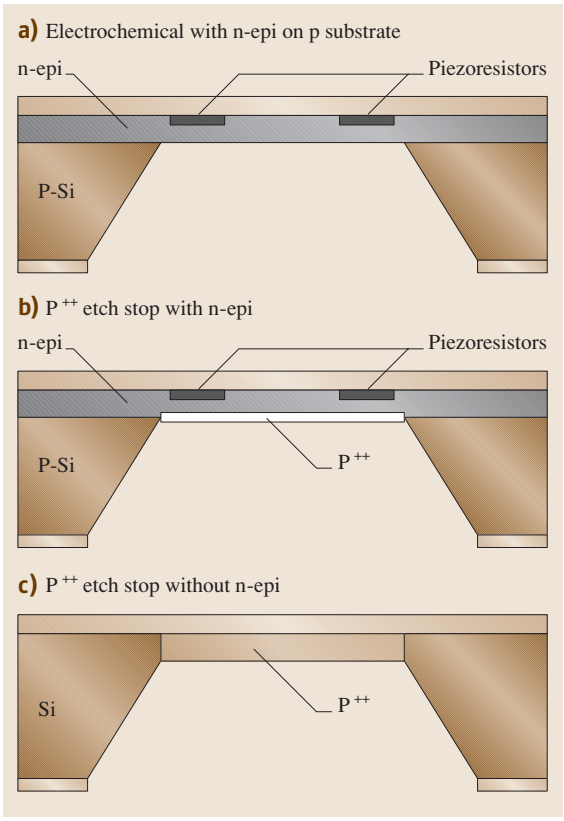


Fig. 7.19 Wet anisotropic silicon back-side etching

Bulk Micromachining Using Wet Etch and Wafer Bonding

The first use of anisotropic wet etchants to remove silicon is often used to mark the beginning of the micromachining era. Back-side etch was used to create movable structures such as beams, membranes and plates, see Fig. 7.19. Initially, the etching was timed in order to create a specified thickness. However, this technique proved to be inadequate for creating thin structures ($<20\,\mu m$). Subsequent use of various etch stop techniques allowed the creation of thinner membranes in a more controlled fashion. As was mentioned in Sect. 7.1.3, the use of heavily doped boron regions and electrochemical bias can drastically slow down the etch process and hence create microstructures with controllable thicknesses. Figure 7.20a,b shows the cross-section of two piezoresistive pressure sensors fabricated using electrochemical and P^{++} etch stop techniques. The P^{++} method requires the epitaxial growth of a lightly doped region on top of a P^{++} etch stop layer. This layer is subsequently used for the placement of piezoresistors. However, if no active component is required, one can simply use the P^{++} region to create a thin membrane, Fig. 7.20c.

The P^{++} etch stop technique can also be used to create isolated thin silicon structures via the dissolu-



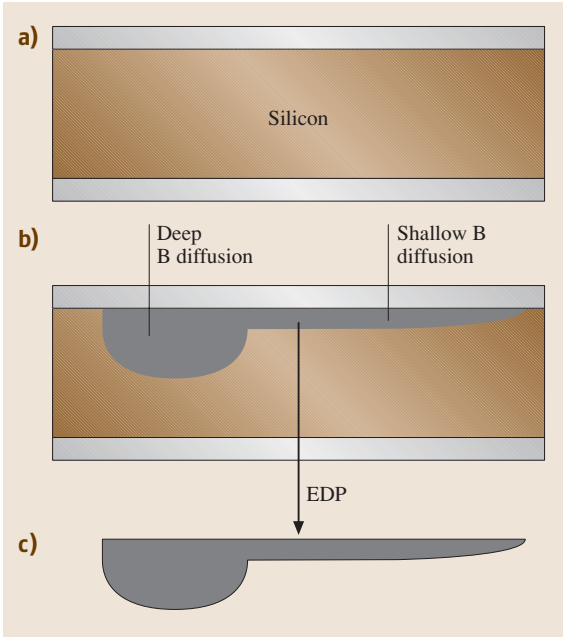


Fig. 7.20a–c Wet micromachining etch stop techniques: **(a)** electrochemical with n-epi on p substrate, **(b)** P^{++} etch stop with n-epi, and **(c)** P^{++} etch stop without n-epi ◀

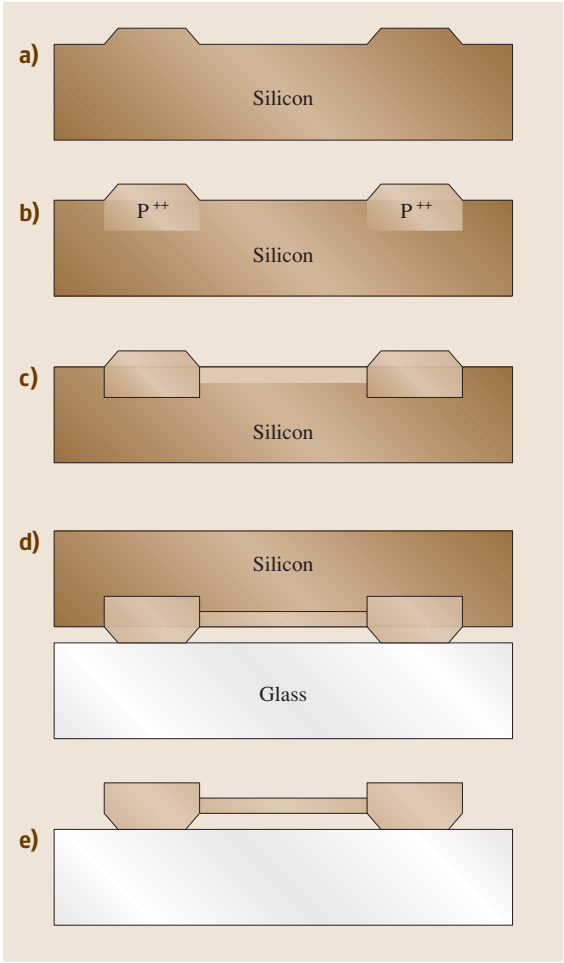


Fig. 7.22a–e Dissolved wafer process sequence: **(a)** KOH etch, **(b)** deep B diffusion, **(c)** shallow B diffusion, **(d)** silicon–glass anodic bond, and **(e)** release in EDP

tion of the entire lightly doped region [7.19]. This technique was successfully used to fabricate silicon recording and stimulating electrodes for biomedical applications. Figure 7.21 shows the cross-section of one such process which relies on deep (15–20 μm) and shallow boron (2–5 μm) diffusion steps to create microelectrodes with flexible connecting ribbon cables. An

Fig. 7.21 Free-standing microstructure fabrication using deep and shallow boron diffusions and EDP release

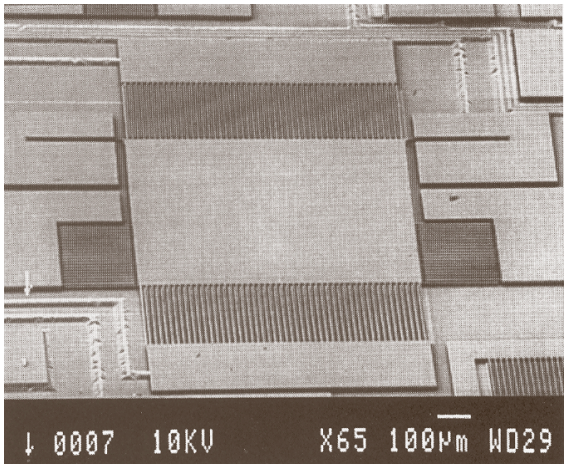


Fig. 7.23 SEM photograph of a microaccelerometer fabricated using the dissolved wafer process [7.20]

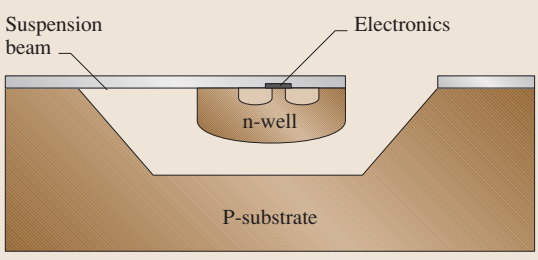


Fig. 7.24 Suspended island created on a prefabricated CMOS chip using front-side wet etch and an electrochemical etch stop

extension of this process which uses a combination of P^{++} etch stop layers and silicon–glass anodic bonding has also been developed. This process is commonly known as the dissolved wafer process and has been used to fabricate a variety of microsensors and microactuators [7.20]. Figure 7.22 shows the cross-section for this process. Figure 7.23 shows an SEM photograph of a microaccelerometer fabricated using the dissolved wafer process.

It is also possible to merge wet bulk micromachining and microelectronics fabrication processes to build micromechanical components on the same substrate as the integrated circuits (CMOS, Bipolar, or BiCMOS) [7.21]. This is very appealing since it allows the integration of interface and signal processing circuitry with MEMS structures on a single chip. However, important fabrication issues such as process compatibility and yield must be considered carefully. One of the most popular techniques in this category is the postprocessing of CMOS integrated circuits by frontside etching in TMAH solutions. As was mentioned previously, silicon-rich TMAH does not attack aluminium and it can therefore be used to undercut microstructures into a preprocessed CMOS chip. Figure 7.24 shows a schematic of this process, where a frontside wet etch and electrochemical etch stop have been used to produce suspended beams. This technique has been used extensively to fabricate a variety of microsensors (including humidity, gas, chemical and pressure microsensors). Figure 7.25 shows a photograph of a post-CMOS-processed chemical sensor.

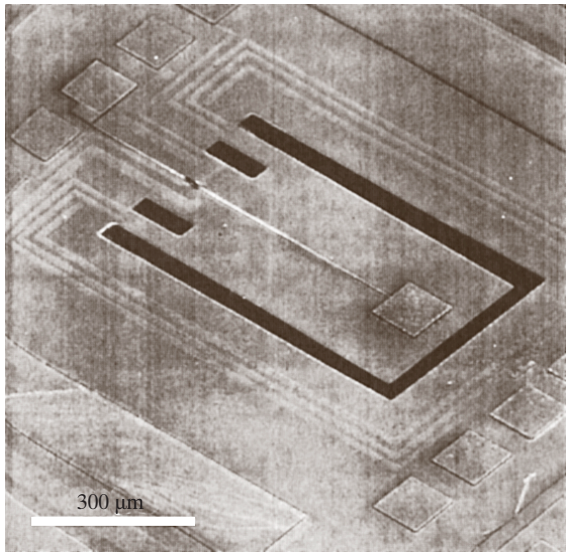


Fig. 7.25 Photograph of a post-CMOS-processed cantilever beam resonator for chemical sensing [7.21]

Bulk Micromachining Using Dry Etch

Bulk silicon micromachining using dry etch is a very attractive alternative to the wet techniques described in the previous section. These techniques were developed during the mid-1990s following the successful development of anisotropic dry silicon etch processes. More recent advances in deep silicon RIE and the availability of SOI wafers with a thick top silicon layer have increased the applications of these techniques. They allow the fabrication of vertical structures with high aspect ratios in isolation or along with on-chip electronics. Process compatibility with active microelectronics is less of a concern for dry methods since many of them do not damage the circuit or its interconnect.

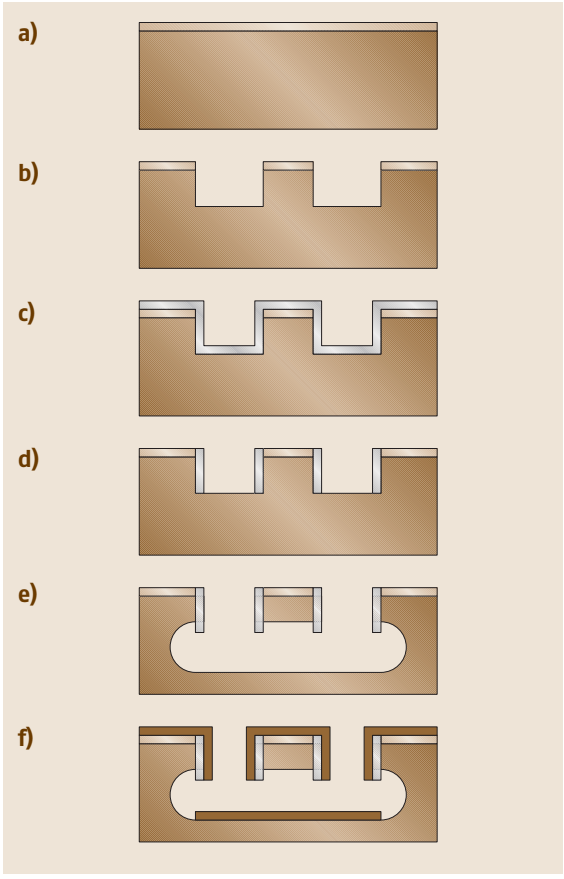


Fig. 7.26 Cross-section of the SCREAM process

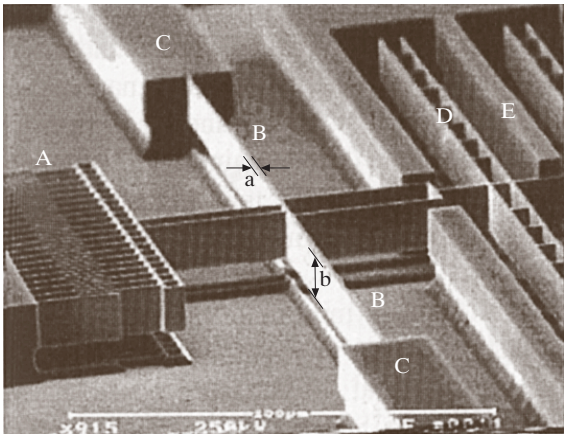


Fig. 7.27a–e SEM photographs of structures fabricated using the SCREAM process: **(a)** comb-drive actuator, **(b)** suspended spring, **(c)** spring support, **(d)** moving suspended capacitor plate, and **(e)** fixed capacitor plate [7.25]

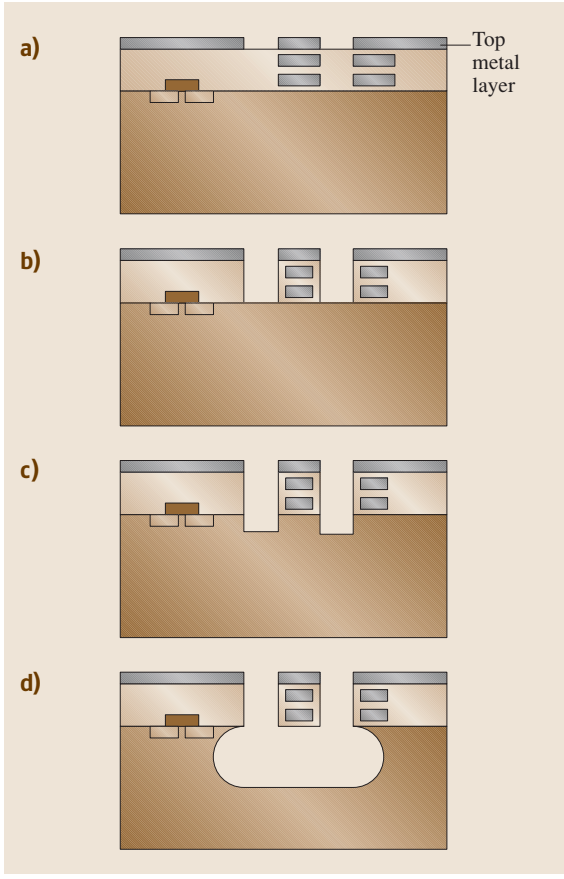


Fig. 7.28 Cross-section of the process flow for post-CMOS dry microstructure fabrication

The most simple dry bulk micromachining technique relies on the frontside undercutting of microstructures using XeF_2 vapor phase etch [7.22]. However, as was mentioned before, this is an isotropic etch and so it has limited applications. A combination of isotropic/anisotropic dry etch is more useful and can be used to create a variety of interesting structures. Two successful techniques using this combination are single-crystal reactive etching and metallization (SCREAM) [7.23] and post-CMOS dry release using aluminium/silicon dioxide laminate [7.24]. The first technique relies on the combination of isotropic/anisotropic dry etch to create single-crystalline suspended structures. Figure 7.26 shows a cross-section of the process. It starts with an anisotropic (Cl_2/BCl_3) silicon etch using an oxide mask (Fig. 7.26b). This is followed by conformal PECVD oxide deposition (Fig. 7.26c). Then an anisotropic oxide etch is used

to remove the oxide at the bottom of the trenches, leaving the sidewall oxide intact (Fig. 7.26d). At this stage an isotropic silicon etch (SF_6) is performed, which results in undercutting and the release of the silicon structures (Fig. 7.26e). Finally, if electrostatic actuation is desired, a metal can be sputtered to cover the top and sidewall of the microstructure and the bottom of the cavity formed below it (Fig. 7.26f). Figure 7.27 shows an SEM photograph of a comb-drive actuator fabricated using SCREAM technology.

The second dry release technique relies on the masking ability of aluminium interconnect lines in a CMOS integrated circuit in order to create suspended microstructures. Figure 7.28 shows a cross-section of this process. As can be seen, the third level Al of a prefabricated CMOS chip is used as a mask to anisotropically etch the underlying oxide layers all the way to the silicon (CHF_3/O_2), Fig. 7.28b. This is followed by an anisotropic silicon etch to create a recess in the silicon which will be used in the final step to facilitate the undercut and release Fig. 7.28c. Finally, an isotropic silicon etch is used to undercut and release the structures, see Fig. 7.28d. Figure 7.29 shows an SEM photograph of a comb-drive actuator fabricated using this technology.

In addition to the methods described above, recent advancements in the development of deep reactive ion etching of silicon (DRIE, see Sect. 7.1.3) have created new opportunities for dry bulk micromachining techniques (see Sect. 7.2.3). One of the most important ones uses thick silicon SOI wafers which are commercially available in various top silicon thicknesses [7.27]. Figure 7.30 shows the cross-section of a typical process that uses DRIE and SOI wafers. The top silicon layer is patterned and etched all the way to the buried oxide,

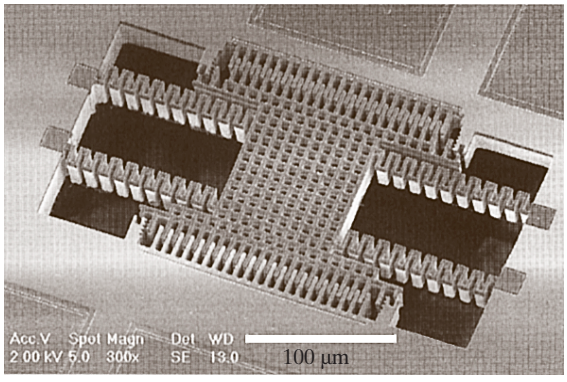


Fig. 7.29 SEM photograph of a comb-drive actuator fabricated using aluminium mask post-CMOS dry release [7.26]

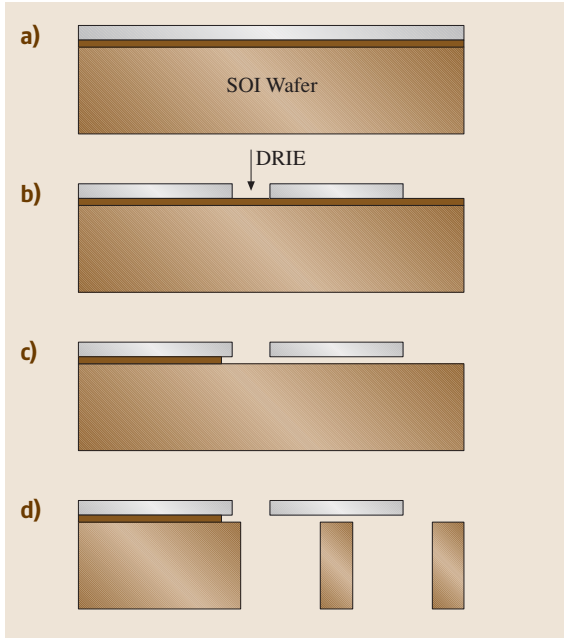


Fig. 7.30 DRIE processes using SOI wafers

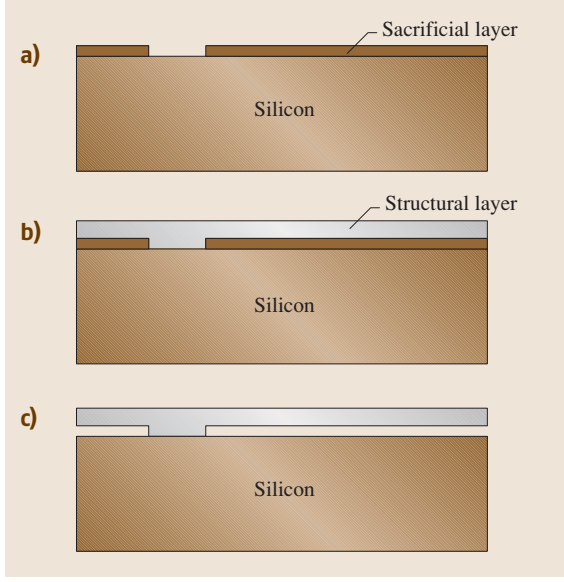


Fig. 7.31 Basic surface micromachining fabrication process

Fig. 7.31b. The oxide is subsequently removed in HF, releasing suspended single-crystalline microstructures, see Fig. 7.31c. In a modified version of this process, the substrate can also be removed from the back-side, al-

lowing easy access from both sides (this makes release easier and prevents stiction), see Fig. 7.31d.

7.2.2 Surface Micromachining

Surface micromachining is another important MEMS microfabrication technique that can be used to create movable microstructures on top of a silicon substrate [7.28]. This technique relies on the deposition of structural thin films on a sacrificial layer which is subsequently etched away resulting in movable micromechanical structures (beams, membranes, plates, and so on). The main advantage of surface micromachining is that extremely small sizes can be obtained. In addition, it is relatively easy to integrate the micromachined structures with on-chip electronics for increased functionality. However, due to the increased surface nonplanarity with any additional layer, there is a limit to the number of layers that can be deposited. Although one of the earliest reported MEMS structures was a surface-micromachined resonant gate transistor [7.29], material-related difficulties resulted in the termination of efforts in this area. In the mid 1980s, improvements in the field of thin film deposition rekindled interest in surface micromachining [7.30]. Polysilicon surface micromachining was introduced later on in the same decade, which opened the door to the fabrication of a variety of microsensors (including accelerometers and gyroscopes) and microactuators (micromirrors, RF switches, and so on). In this section, we will concentrate on the key process steps involved in surface micromachining fabrication and the various materials used in the surface micromachining process. We will also discuss the monolithic integration of CMOS with MEMS structures and 3-D surface micromachining.

Basic Surface Micromachining Processes

The basic surface micromachining process is illustrated in Fig. 7.31. The process begins with a silicon substrate on top of which a sacrificial layer is grown and patterned, Fig. 7.31a. The structural material is then deposited and patterned, Fig. 7.31b. As can be seen, the structural material is anchored to the substrate through the openings created in the sacrificial layer during the previous step. Finally, the sacrificial layer is removed, resulting in the release of the microstructures Fig. 7.32c. In wide structures, it is usually necessary to provide access holes in the structural layer for fast sacrificial layer removal. It is also possible to seal microcavities created by the surface micromachining technique [7.10]. This can be done at the wafer level and is a big advantage in applications such as pressure sensors which require a sealed cavity. Figure 7.32 shows two different techniques that can be used for this purpose. In the first technique, following the etching of the sacrificial layer, a LPCVD dielectric layer (oxide or nitride) is deposited to cover and seal the etch holes in the structural material, Fig. 7.33a. Since the LPCVD deposition is performed at reduced pressures, a subatmospheric pill-box microcavity can be created.

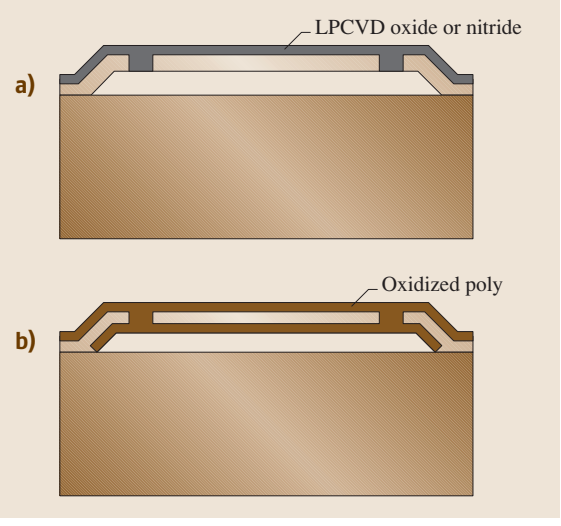


Fig. 7.32 Two sealing techniques for cavities created by surface micromachining

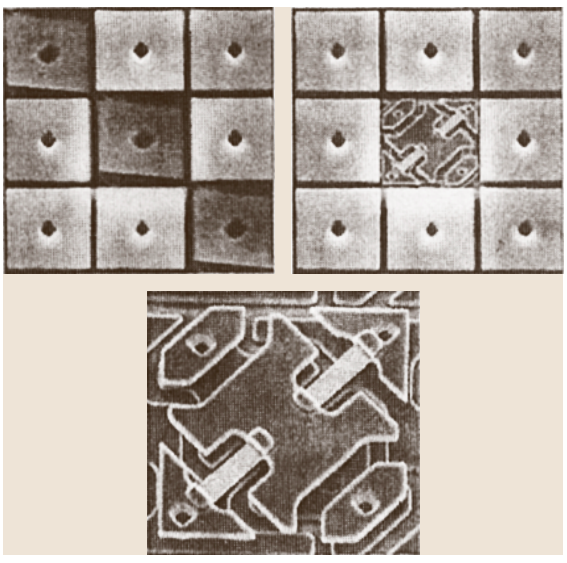


Fig. 7.33 SEM photographs of Texas Instrument's micromirror array [7.28]

In the second technique, also called "reactive sealing", the polysilicon structural material is oxidized following the removal of the sacrificial layer, Fig. 7.33b. If the access holes are small enough, the grown oxide can seal the cavity. Due to the consumption of oxygen during the growth process, the cavity is also subatmospheric in this case.

The most common sacrificial and structural materials are phosphosilicate glass (PSG) and polysilicon, respectively (low temperature oxide or LTO is also frequently used as the sacrificial layer). However, there are several other sacrificial/structural combinations that have been used to create a variety of surface micromachined structures. Important design issues related to the choice of the sacrificial layer are: 1) quality (pinholes and so on), 2) ease of deposition, 3) deposition rate, 4) deposition temperature, and 5) etch difficulty and selectivity (the sacrificial layer etchant should not attack the structural layer). The particular choice of material used for the structural layer depends on the desired properties and specific application. Several important requirements are: 1) ease of deposition, 2) deposition rate, 3) step coverage, 4) mechanical properties (internal stress, stress gradient, Young's moduli, fracture strength and internal damping), 5) etch selectivity, 6) thermal budget and history, 7) electrical conductivity, and 8) optical reflectivity. Two examples from the commercially available surface micromachined devices illustrate various successful sacrificial/structural combinations. Texas Instruments (TI; Dallas, TX) deformable mirror display (DMD) spatial light modulators uses aluminium as the structural material (good optical reflectivity) and photoresist as the sacrificial layer (easy dry etch and low processing temperatures, allowing easy post-IC integration with CMOS) [7.32], Fig. 7.33, whereas Analog Devices' (Cambridge, MA) microgyroscope uses polysilicon structural material and a PSG sacrificial layer, Fig. 7.34. Two recent additions to the collection of available structural layers are polysilicon-germanium and polygermanium [7.33, 34]. These are intended for use as substitutes for polysilicon in applications where the high polysilicon deposition temperature (around 600 °C) is prohibitive (during CMOS integration for example). Unlike LPCVD polysilicon, polygermanium (poly-Ge) and polysilicon-germanium (poly-$Si_{1-x}Ge_x$) can be deposited at temperatures as low as 350 °C (the poly-Ge deposition temperature is usually lower than poly-SiGe). Table 7.2 summarizes important surface micromachined sacrificial/structural combinations.

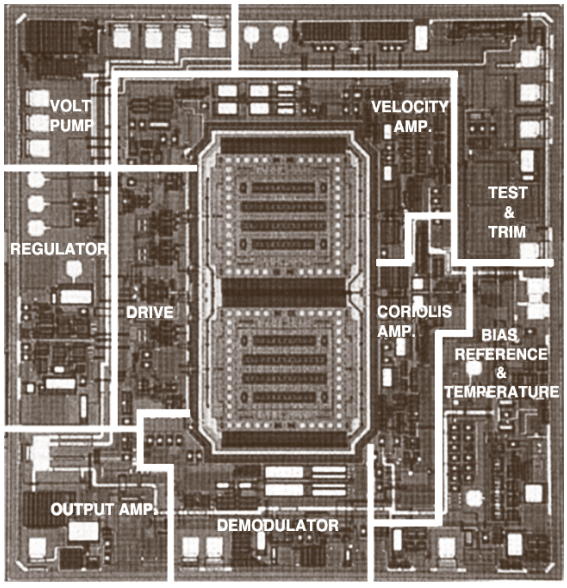


Fig. 7.34 SEM photograph of Analog Devices' gyroscope [7.31]

An important consideration in the design and processing of surface micromachined structures is the issue of stiction [7.10, 35, 36]. This can happen during the release step if a wet etchant is used to remove the sacrificial layer or during the device lifetime. The reason for stiction during release is the surface tension of the liquid etchant, which can hold the microstructure down and cause stiction. This usually happens when the structure is compliant and does not possess a strong enough spring constant to overcome the surface tension force of the rinsing liquid (water). There are several ways to alleviate the release-related stiction problem.

Table 7.2 Several important surface-micromachined sacrificial/structural combinations

System	Sacrificial layer	Structural layer	Structural layer etchant	Sacrificial layer etchant
1	PSG or LTO	Poly-Si	RIE	Wet or vapor HF
2	Photoresist, polyimide	Metals (Al, Ni, Co, Ni-Fe)	Various metal etchants	Organic solvents, plasma O_2
3	Poly-Si	Nitride	RIE	KOH
4	PSG or LTO	Poly-Ge	H_2O_2 or RCA1	Wet or vapor HF
5	PSG or LTO	Poly-Si-Ge	H_2O_2 or RCA1	Wet or vapor HF

These include: 1) the use of dry or vapor phase etchant, 2) the use of solvents with lower surface tensions, 3) geometrical modifications, 4) CO_2 critical drying, 5) freeze-drying, and 6) self-assembled monolayer (SAM) or organic thin film surface modification. The first technique prevents stiction by circumventing the need for a wet etchant, although in condensation is a possibility in the case of vapor phase release, which can also cause some stiction. The second method uses a rinsing solvent (such as methanol) that has a lower surface tension than water. This is usually followed by rapid evaporation of the solvent using a hot-plate. However, this is not the best technique, because many structures still stick. The third technique is geometrical; dimples are placed in the structural layer in order to reduce the contact surface area and hence reduce the attractive force. The fourth and fifth techniques rely on a phase change (of CO_2 in one case and butyl-alcohol in the other) which avoids the liquid phase altogether by jumping directly to the gas phase. The last technique uses self-assembled monolayers or organic thin films to coat the surfaces with a hydrophobic layer. The stiction that occurs during the operating lifetime of the device (in-use stiction) is due to the condensation of moisture on surfaces, electrostatic charge accumulation, or direct chemical bonding. Surface passivation using self-assembled monolayers or organic thin films can be used to reduce the surface energy and to reduce or eliminate the capillary forces and direct chemical bonding. These organic coatings also reduce electrostatic forces if a thin layer is applied directly to the semiconductor (without the intervening oxide layer). Commonly used organic coatings include fluorinated fatty acids (TI's aluminium micromirrors), silicone polymeric layers (Analog Devices' accelerometers) and siloxane self-assembled monolayers.

Surface Micromachining Integration with Active Electronics

Integration of surface micromachined structures with on-chip circuitry can increase performance and simplify packaging. However, issues related to process compatibility and yield must be considered carefully. The two most common techniques are MEMS-first and MEMS-last techniques. In the MEMS-last technique, the integrated circuit is fabricated and surface micomachined structures are subsequently built on top of the silicon wafer. An aluminium structural layer with a photoresist sacrificial layer is an attractive combination due to the low thermal budget of the process (TI'S micromirror array). However, in applications where the mechanical properties of Al are not adequate, polysilicon structural material must be used with a sacrificial layer of LTO or PSG. Due to the rather high deposition temperature of polysilicon, this combination requires that special attention is paid to the thermal budget. For example, aluminium metallization must be avoided and substituted with refractory metals such as tungsten. This can only be achieved at the cost of greater process complexity and lower transistor performance.

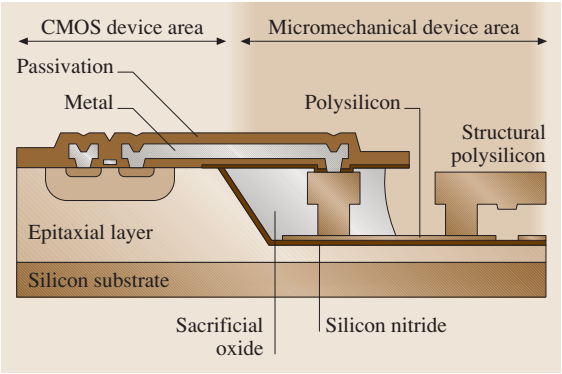


Fig. 7.35 Cross-section of the Sandia MEMS-first integrated fabrication process

The MEMS-first technique alleviates these difficulties by fabricating the microstructures at the very beginning of the process. However, if the microstructures are processed first, they must be buried in a sealed trench to eliminate interference with microstructures from subsequent CMOS processes. Figure 7.35 shows a cross-section of a MEMS -first fabrication process developed at the Sandia National Laboratory [7.37]. The process starts with a shallow anisotropic etching of trenches in a silicon substrate to accommodate the height of the polysilicon structures fabricated later on. A silicon nitride layer is then deposited to provide isolation at the bottom of the trenches. Next, several layers of polysilicon and sacrificial oxide are deposited and patterned in a standard surface micromachining process. Then the trenches are completely filled with sacrificial oxide and the wafers are planarized with chemical-mechanical polishing (this avoids any complications in the following lithographic steps). After an annealing step, the trenches are sealed with a nitride cap. At this point, a standard CMOS fabrication process is performed. At the end of the CMOS process, the nitride cap is etched and the buried structures are released by etching the sacrificial oxide.

3-D Microstructures From Surface Micromachining

3-D surface microstructures can be fabricated using surface micromachining. The fabrication of hinges used in the vertical MEMS assembly was a major step towards achieving 3-D microstructures [7.39]. Optical microsytems have greatly benefited from surface-micromachined 3-D structures. These microstructures are used as passive or active components (micromirror, Fresnel lens, optical cavity, and so on) on a silicon optical bench (silicon microphotonics). One example is a Fresnel lens that has been surface micromachined in polysilicon and then erected using hinge structures and locked in place using micromachined tabs, thus liberating the structure from the horizontal plane of the wafer [7.38, 40]. Various microactuators (such as comb-drive and vibromotors) have been used to move these structures out of the silicon plane and into position. Figure 7.36 shows an SEM photograph of a bar-code microscanner that uses a silicon optical microbench with 3-D surface micromachined structures.

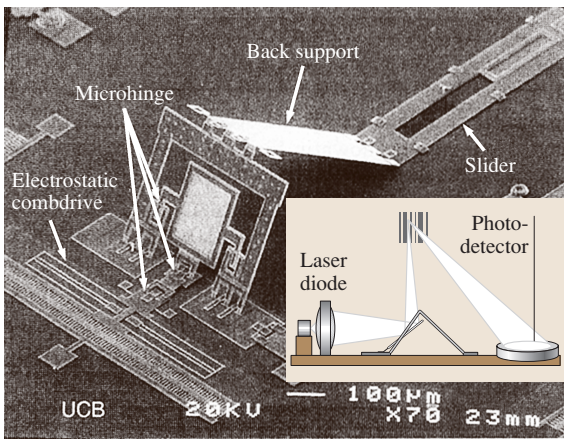


Fig. 7.36 Silicon pin-and-sample hinge scanner with 3-D surface micromachined structures [7.38]

7.2.3 High Aspect Ratio Micromachining

The bulk and surface micromachining technologies presented in the previous sections fulfill the requirements of a large group of applications. Certain applications, however, require the fabrication of high aspect ratio structures that cannot be realized with the aforementioned technologies. In this section we describe three technologies – LIGA, HEXSIL and HARPSS– which are capable of producing structures that have vertical dimensions that are much larger than their lateral dimensions via X-ray lithography (LIGA) and DRIE etching (HEXSIL and HARPSS).

LIGA

LIGA is a high aspect ratio micromachining process that relies on X-ray lithography and electroplating (in German: Lithographie galvanoformung abformung) [7.41, 42]. We have already introduced the concept of the plating-through-mask technique (in Sect. 7.1.2; see Fig. 7.10). With standard UV photolithography and photoresists, the maximum thickness achievable is on the order of a few tens of microns and the resulting metal structures show tapered walls. LIGA is a technology based on the same plating-through-mask idea but it can be used to fabricate metal structures with thicknesses of a few microns to a few millimeters with almost vertical sidewalls. This is achieved using X-ray lithography and special photoresists. Due to their short wavelengths, X-rays are capable of penetrating through a thick photoresist layer with no scattering and of defining features with lateral dimensions down to 0.2 µm (aspect ratio $> 100{:}1$).

The photoresists used in LIGA should comply with certain requirements, including sensitivity to X-rays, resistance to electroplating chemicals, and good adhesion to the substrate. Based on such requirements, poly-(methylmethacrylate) (PMMA) is considered to be an optimal choice for the LIGA process. Application of the thick photoresist on top of the substrate can be performed by various techniques, such as multiple spin-coating, precast PMMA sheets, and plasma polymerization coating. The mask structure and materials used for X-ray lithography must also comply with certain requirements. The traditional masks based on glass plates with a patterned chrome thin layer are not suitable because X-rays are not absorbed by the chromium layer and the glass plate is not transparent enough. Instead, X-ray lithography uses a silicon nitride mask with gold as the absorber material (typically formed by electroplating gold to a thickness of 10–20 µm). The nitride membrane is supported by a silicon frame which can be fabricated using bulk micromachining techniques. Once the photoresist is exposed to the X-rays and developed, the process proceeds with the electroplating of the desired metal. Ni is the most common, although other metals and metallic compounds such us Cu, Au, NiFe, and NiW are also electroplated in LIGA processes. A good agitation of the plating solution is the key to obtaining a uniform and repeatable result during this step. A paddle plating cell, based on a windshield-wiper-like

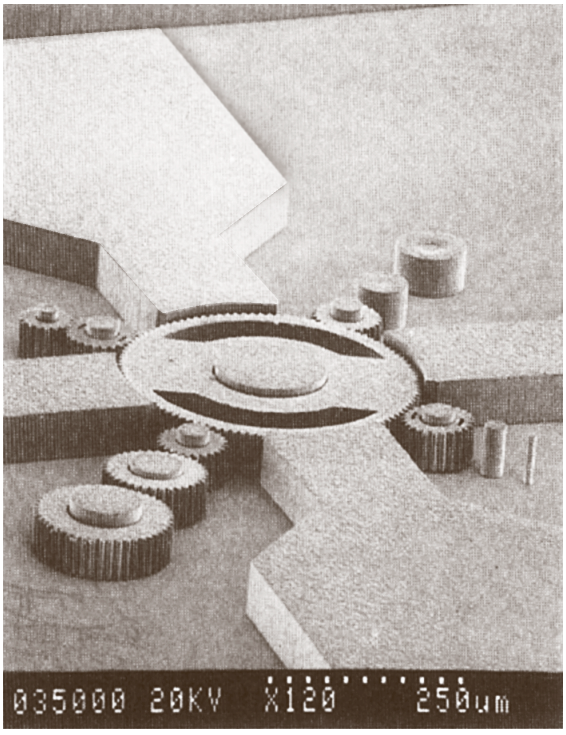


Fig. 7.37 SEM of assembled LIGA-fabricated nickel structures [7.42]

device moving only a millimeter away from the substrate surface, provides extremely reproducible agitation. Figure 7.37 shows an SEM of a LIGA microstructure fabricated by electroplating nickel.

Due to the expensive nature of X-ray sources (related to synchrotron radiation), LIGA technology was initially intended for the fabrication of molds that could be used many times in hot embossing or injection molding processes. However, it has been also used in many applications to form high aspect ratio metal structures directly on top of a substrate. A cheaper alternative to the LIGA process (although somewhat poorer quality) called UV-LIGA or "poor man's LIGA" has been proposed [7.43, 44]. This process uses SU-8 negative photoresists (available for spin-coating at various thickness ranging from 1 to 500 μm) and standard contact lithography equipment. Aspect ratios larger than 20:1 have been demonstrated using this technique. A major problem with this alternative is the removal of the SU-8 photoresist after plating. Various methods have been proposed with different degrees of success. These include: wet etching with special solvents; burning at high tem-

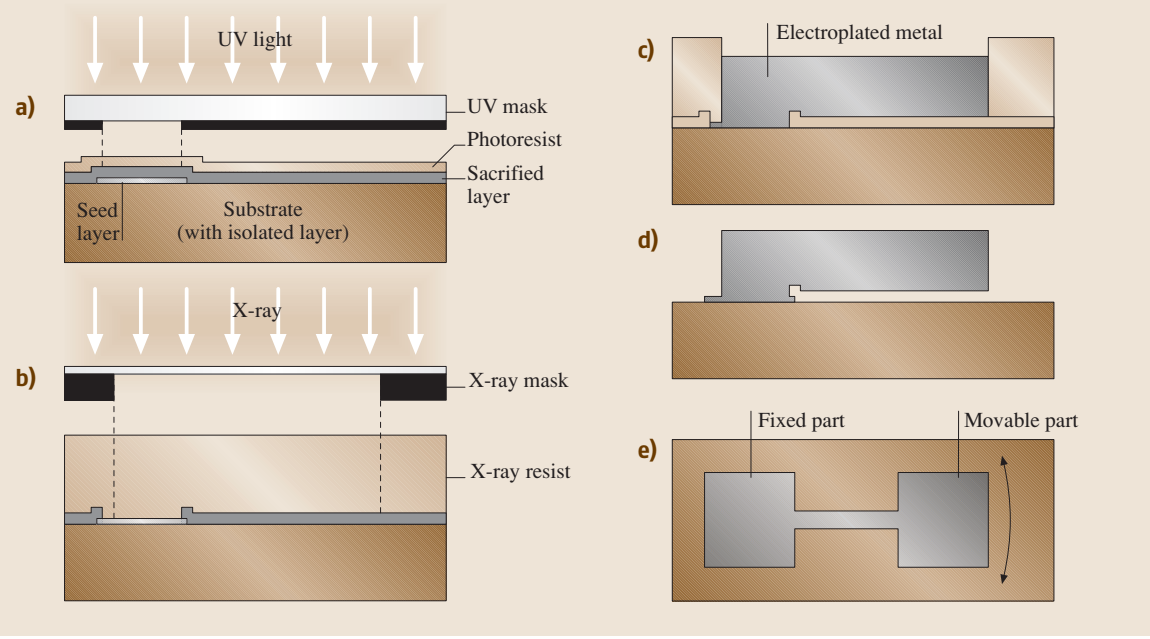


Fig. 7.38a–e Sacrificial LIGA process: **(a)** UV lithography for sacrificial layer patterning, **(b)** X-ray lithography, **(c)** electroplating, **(d)** structure release, **(e)** top view of the movable structure

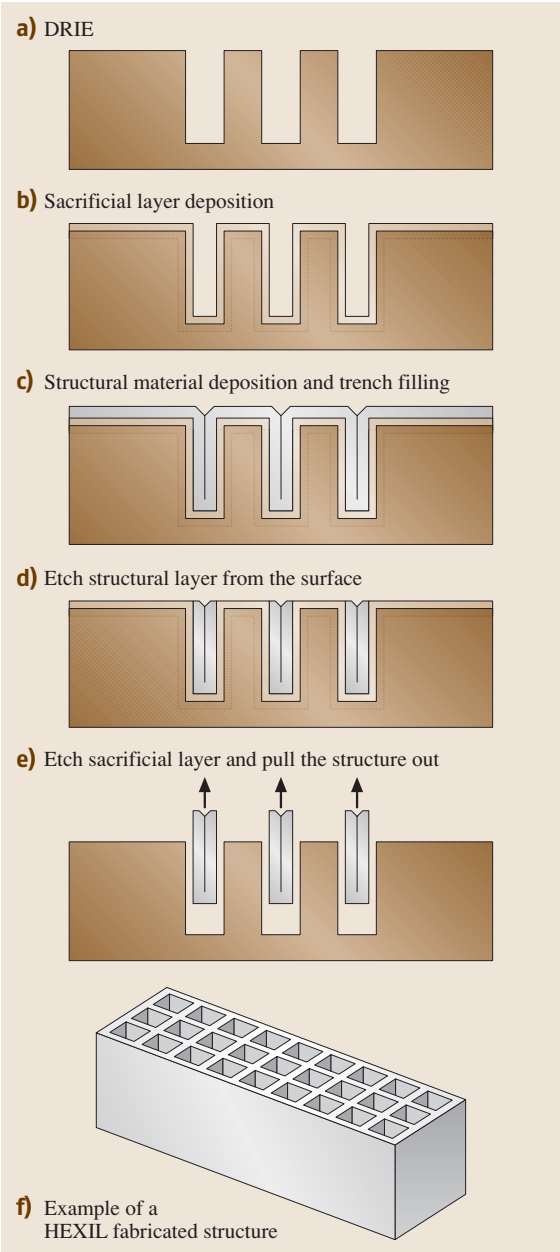


Fig. 7.39a–f HEXSIL process flow: (**a**) DRIE, (**b**) sacrificial layer deposition, (**c**) structural material deposition and trench filling, (**d**) etch structural layer from the surface, (**e**) etch sacrificial layer and pull the structure out, (**f**) example of a HEXSIL fabricated structure

peratures (600 °C); dry etching; use of a release layer; and high-pressure water jet etching.

A variation on the basic LIGA process, shown in Fig. 7.38, permits the fabrication of electrically isolated movable structures, and thus opens up more possibilities for sensor and actuator design using this technology [7.46]. This so-called "sacrificial LIGA" (SLIGA) starts with the patterning of the seed layer. A sacrificial layer (such as titanium) is then deposited and patterned. The process then proceeds as usual in standard LIGA until the last step, when the sacrificial layer is removed. The electroplated structures that overlap with the sacrificial layer are released in this step.

HEXSIL

The second method for fabricating high aspect ratio structures, which is based on a template replication technology, is HEXSIL (HEXagonal honeycomb polySILicon) [7.47]. Figure 7.39 shows a simplified process flow. A high aspect ratio template is first formed in a silicon substrate using DRIE. Then a sacrificial multilayer is deposited to allow the final release of the structures. The multilayer is composed of one or more PSG nonconformal layers, used for fast etch release (≈20 μm/min in 49% HF), alternated with conformal layers of either oxide or nitride to provide enough thickness for proper release of the structures. The total thickness of the sacrificial layer must be larger than the shrinkage or elongation of the structures caused by the relaxation of the internal stress (compressive or tensile) during the release step, otherwise the structures will clamp themselves to the walls of the template and retrieval will not be possible. Any material that can be conformally deposited and released during the HF

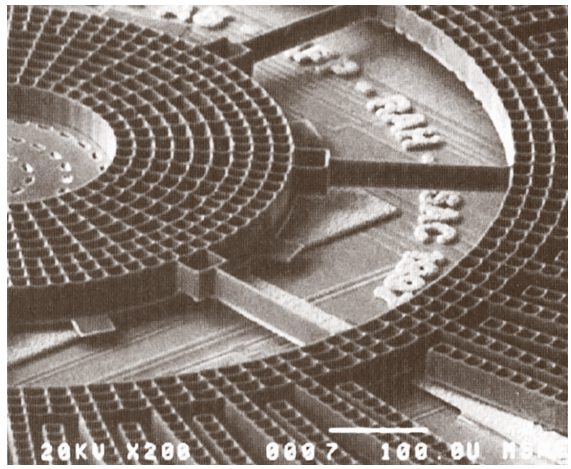


Fig. 7.40 SEM micrograph of an angular microactuator fabricated using HEXSIL [7.45]

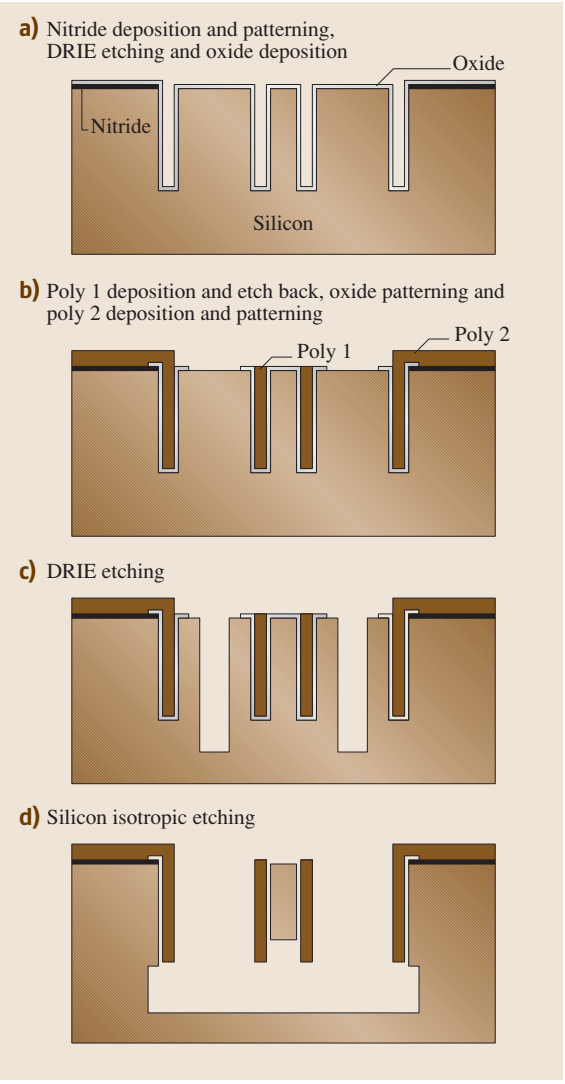


Fig. 7.41a–d HARPSS process flow: **(a)** nitride deposition and patterning, DRIE etching and oxide deposition, **(b)** poly 1 deposition and etch back, oxide patterning and poly 2 deposition and patterning, **(c)** DRIE etching, **(d)** silicon isotropic etching

release step without damage is suitable for the structural layer. Structures made of polysilicon, nitride, and electroless nickel [7.48] have been reported. Nickel can only be deposited in combination with polysilicon since a conductive surface is needed for the deposition to occur. After the deposition of the structural materials, a blanket etch (poly or nitride) or a mechanical lapping (nickel) is performed to remove the excess material from the surface. Finally, 49% HF with surfactant is used to dissolve the sacrificial layers. The process can be repeated many times using the same template, which lowers the fabrication costs considerably. Figure 7.40 shows an SEM photograph of a microactuator fabricated using the HEXSIL process.

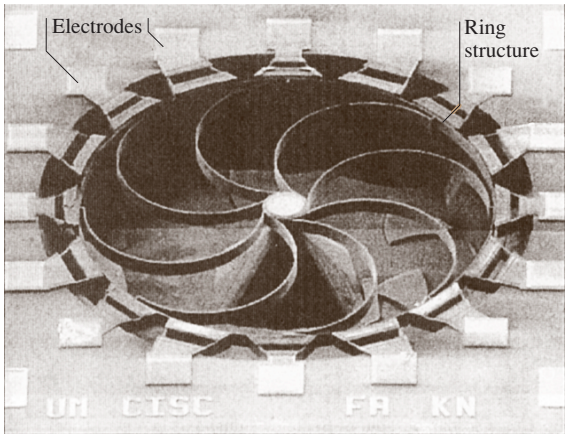


Fig. 7.42 SEM photograph of a microgyroscope fabricated using the HARPSS process [7.49]

HARPSS

The High Aspect Ratio combined Poly- and Single-crystal Silicon (HARPSS) technology is another technique capable of producing high aspect ratio electrically isolated polycrystalline and single-crystal silicon microstructures with capacitive air gaps ranging in size from submicrometer to tens of micrometers [7.50]. The structures, tens to hundreds of micrometers thick, are defined by trenches etched with DRIE and are filled with oxide and poly layers. The release of the microstructures is achieved at the end by means of a directional silicon etch followed by an isotropic etch. The small vertical gaps and thick structures possible with this technology find application during the fabrication of a variety of MEMS devices, particularly inertial sensors [7.51] and RF beam resonators [7.52]. Figure 7.41 shows the process flow at the cross-section of a single-crystal silicon beam resonator. The HARPSS process starts with the deposition and patterning of a silicon nitride layer that will be used to isolate the poly structure's connection pads from the substrate. High aspect ratio trenches ($\approx 5\,\mu m$ wide) are then etched into the substrate using a DRIE etcher. Then a conformal oxide layer (LPCVD) is deposited. This layer has two functions: 1) to protect the structures during

the dry etch release, and 2) to define the submicrometer gap between the silicon and polysilicon structures. Following the oxide deposition, the trenches are completely filled with LPCVD polysilicon. The polysilicon is etched back and the oxide beneath is patterned to provide anchor points for the structures. A second layer of polysilicon is then deposited and patterned. Finally, the structures are released using a DRIE step followed by an isotropic silicon etch through a photoresist mask that exposes only the areas of silicon substrate surrounding the structures. It should be noted that single-crystal silicon structures are not protected at the bottom during the isotropic etch. This causes the single-crystal silicon structures to be etched vertically from the bottom, and so they are shorter than the polysilicon structures. Figure 7.42 shows an SEM photograph of a microgyroscope fabricated using the HARPSS process.

7.3 Nanofabrication Techniques

The microfabrication techniques discussed so far are mostly geared towards fabricating devices in the 1 mm to 1 μm size range (although submicron dimensions are possible with certain techniques, such as HARPSS using a dielectric sacrificial layer). Recent years have witnessed a tremendous surge of interest in fabricating submicro- (1 μm-100 nm) and nanostructures (100–1 nm range) [7.53]. This interest arises from both practical and fundamental viewpoints. At the more scientific and fundamental level, nanostructures provide an interesting tool for studying electrical, magnetic, optical, thermal and mechanical properties of matter at the nanometer scale. These include important quantum mechanical phenomena (such as conductance quantization, band-gap modification and coulomb blockade) arising from the confinement of charged carriers in structures such as quantum wells, wires and dots, see Fig. 7.43. On the practical side, employing nanostructures in electronic/optical devices and sensors can lead to significant improvements in performance. In the field of devices, investigators have focused on fabricating nanometer-sized transistors, in anticipation of the predicted technical difficulties with extending Moore's law beyond 100 nm resolution. In addition, optical sources and detectors with nanometer-sized dimensions exhibit enhanced characteristics that are not achievable in larger devices (such as lower threshold currents, improved dynamic behavior, and improved emission line width in quantum dot lasers). These improvements create exciting possibilities for next generation computation and communication devices. In the field of sensing, shrinking dimensions beyond conventional optical lithography can provide major improvements in sensitivity and selectivity.

One can broadly divide various nanofabrication techniques into top-down and bottom-up categories. The first approach starts with a bulk or thin film material and removes selective regions in order to fabricate nanostructures (similar to micromachining techniques). The second method relies on molecular recognition and self-assembly to fabricate nanostructures from smaller building blocks (molecules, colloids and clusters). The top-down approach is obviously an offshoot of standard lithography and micromachining techniques. The bottom-up approach, on the other hand, is more strongly influenced by chemical engineering and material science, and relies on fundamentally different principles. In this chapter, we will discuss five major nanofabrication techniques. These include: i) e-beam and nanoim-

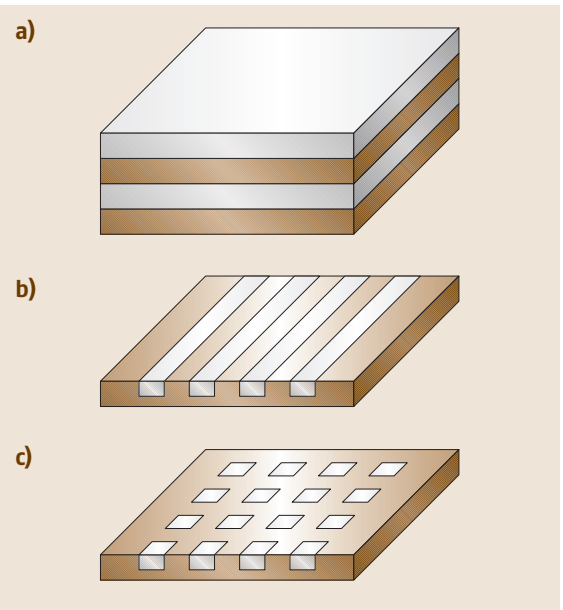


Fig. 7.43a–c Several important quantum confinement structures: **(a)** quantum well, **(b)** quantum wire, and **(c)** quantum dot

print fabrication, ii) epitaxy and strain engineering, iii) scanned probe techniques, iv) self-assembly and template manufacturing, and v) chemical techniques for fabricating nanoparticles and nanowires.

7.3.1 E-Beam and Nanoimprint Fabrication

In previous sections, we discussed several important lithography techniques commonly used in MEMS and microfabrication. These included various forms of UV (regular, deep, and extreme) and X-ray lithographies. However, due to the lack of resolution (in the case of UV) or the difficultlies in manufacturing mask and radiation sources (X-ray), these techniques are not suitable for nanoscale fabrication. E-beam lithography is an alternative and attractive technique for fabricating nanostructures [7.54]. It uses an electron beam to expose an electron-sensitive resist such as polymethyl methacrylate (PMMA) dissolved in trichlorobenzene (positive) or polychloromethylstyrene (negative) [7.55]. The e-beam gun is usually part of a scanning electron microscope (SEM), although transmission electron microscopes (TEM) can also be used. While electron wavelengths of the order of 1 Å are easily achieved, electron scattering in the resist limits the attainable resolutions to >10 nm. The beam control and pattern generation is achieved through a computer interface. E-beam lithography is serial and so it has a low throughput. Although this is not a major concern when fabricating devices used in the study of fundamental microphysics, it severely limits large-scale nanofabrication. E-beam lithography, in conjunction with processes such as lift-off, etching and electro-deposition, can be used to fabricate various nanostructures.

An interesting new technique which circumvents the serial and low throughput limitations of e-beam lithography for fabricating nanostructures is known as nanoimprint technology [7.56]. This technique uses an e-beam-fabricated hard material master (or mold) to stamp and deform a polymeric resist. This is usually followed by a reactive ion etching step to transfer the stamped pattern to the substrate. This technique is economically superior since a single stamp can be used repeatedly to fabricate a large number of nanostructures. Figure 7.44 shows a schematic illustration of nanoimprint fabrication. First, a hard material (such as silicon or SiO_2) stamp is created using e-beam lithography and reactive ion etching. Then a resist-coated substrate is stamped and finally an anisotropic RIE is performed to remove the resist residue in the stamped area. At this stage, the process is complete and one can either etch the substrate, or if metallic nanostructures are desired, evaporate the metal and perform a lift-off.

The resist used in nanoimprint technology can be a thermoplastic, a UV-curable polymer, or a heat-curable

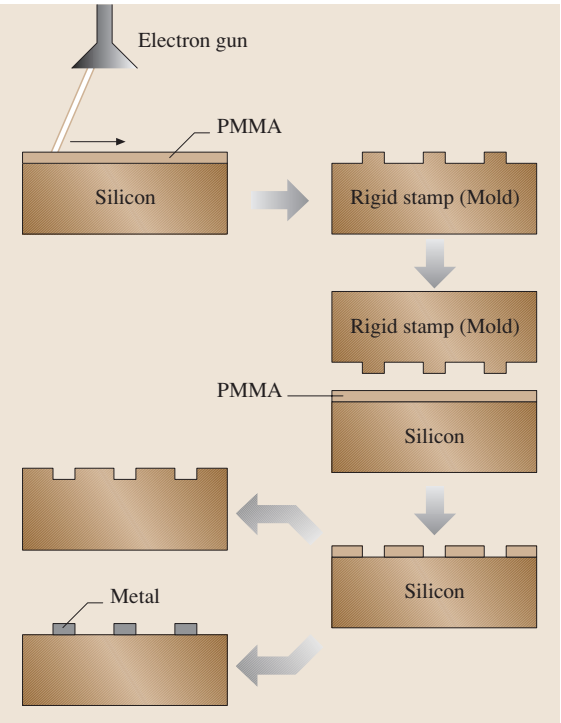


Fig. 7.44 Schematic of nanoimprint fabrication

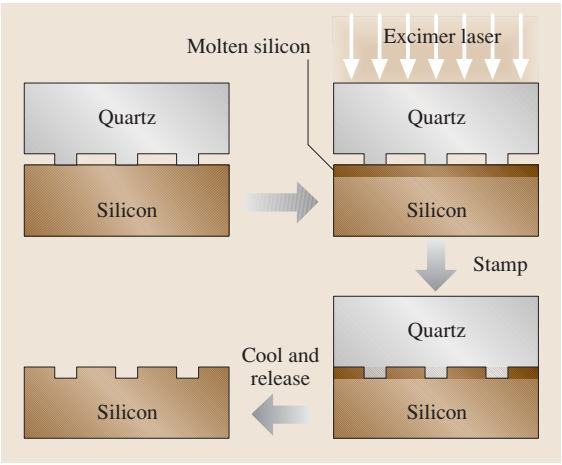


Fig. 7.45 Ultrafast silicon nanoimprinting using an excimer laser

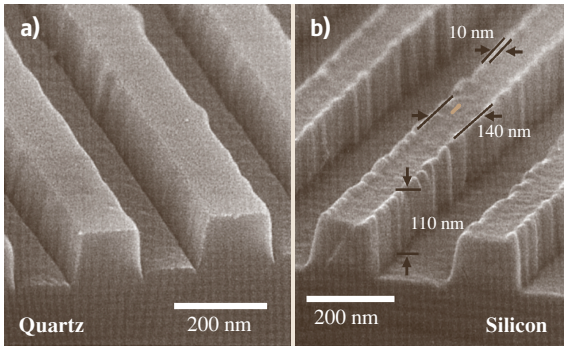


Fig. 7.46a,b SEM micrographs of: **(a)** quartz mold and **(b)**imprinted silicon surface using LADI [7.57]

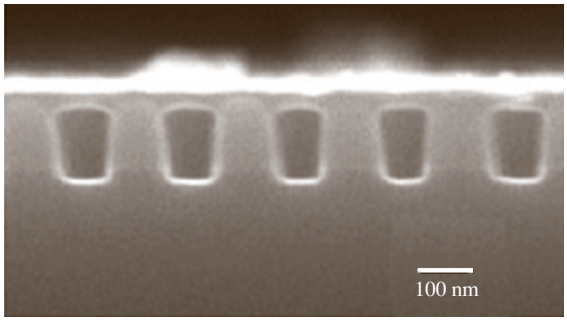


Fig. 7.47 Cross-section of a nanofluidic channel fabricated using nanoimprint lithography [7.60]

polymer. For a thermoplastic resist (such as PMMA), the substrate is heated to above the glass transition temperature (T_g) of the polymer before stamping and is cooled to below T_g before the stamp is removed. Similarly, the UV- and heat-curable resists are fully cured before the stamp is separated. The resolution available from nanoimprint technology is limited by the strength of both the mold and the polymer, and it can be as small as 10 nm. A nanoimprint technique has recently been used to stamp a silicon substrate in less than 250 ns using a XeCl excimer laser (308 nm) and a quartz mask (laser-assisted direct imprint, LADI), Fig. 7.45 [7.57]. Figure 7.46 shows SEM micrographs of the quartz mold and imprinted silicon substrate with 140 nm lines obtained using LADI. Modified nanoimprint lithography processes have also been explored in order to fabricate nanofluidic channels (for DNA manipulation) and multilayer polymeric structures [7.58, 59]. Figure 7.47 shows a cross-section of nanofluidic channels fabricated using nanoimprint lithography. A comprehensive review of this research area by *Guo* [7.60] was recently published.

7.3.2 Epitaxy and Strain Engineering

Atomic precision deposition techniques such as molecular beam epitaxy (MBE) and metallo-organic chemical vapor deposition (MOCVD) have proven to be effective tools for fabricating a variety of quantum confinement structures and devices (including quantum well lasers, photodetectors and resonant tunneling diodes) [7.61–63]. Although quantum wells and superlattices are the structures that lend themselves most easily to these techniques (see Fig. 7.43a), quantum wires and dots have also been fabricated by adding extra steps such as etching and selective growth. The fabrication of quantum well and superlattice structures using epitaxial growth is a mature and well developed field and is therefore not discussed in this section. Instead, we will concentrate on quantum wire and dot nanostructure fabrication using basic epitaxial techniques [7.64, 65].

Quantum Structure Nanofabrication Using Epitaxy on Patterned Substrates

There have been several different approaches to the fabrication of quantum wires and dots using epitaxial layers. The most straightforward technique involves e-beam lithography and etching of an epitaxially grown layer (such as InGaAs on GaAs substrate) [7.66]. However, due to the damage and/or contamination incurred during lithography, this method is not very suitable for active device fabrication (of quantum dot lasers for instance). Several other methods involving the regrowth of epitaxial layers over nonplanar surfaces such as step-edge, cleaved-edge and patterned substrate have been used to fabricate quantum wires and dots without the need for lithography and etching of the quantum-confined structure [7.65, 67]. These nonplanar surface templates can be fabricated in a variety of ways, such as etching through a mask, or cleavage along crystallographic planes. Subsequent epitaxial growth on top of these structures results in a set of planes with different growth rates depending on the geometry or surface diffusion and adsorption effects. These effects can significantly enhance or limit the growth rate on certain planes, resulting in lateral patterning and confinement of deposited epitaxial layers and formation of quantum wires (in V-grooves) and dots (in inverted pyramids). Figure 7.48a shows a schematic cross-section of an InGaAs quantum wire fabricated in a V-groove InP. As can be seen, the growth rate on the sidewalls is lower than that on the top and bottom surfaces. Therefore, the thicker InGaAs layer at the bottom of the V-groove forms a quantum wire confined from the sides by a thin-

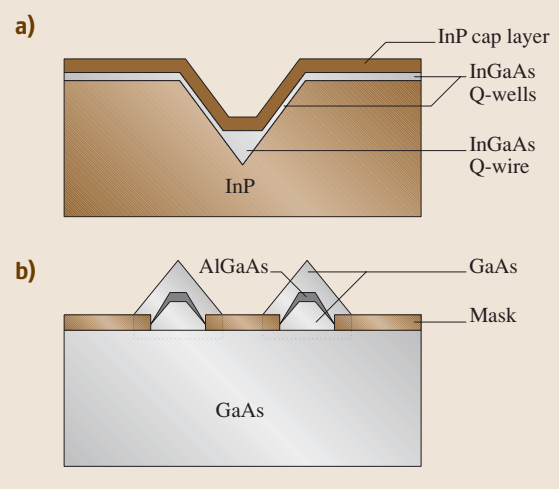


Fig. 7.48 **(a)** InGaAs quantum wire fabricated in a V-groove InP, and **(b)** AlGaAs quantum wire fabricated via epitaxial growth on a masked GaAs substrate

ner layer with a wider band-gap. Figure 7.48b shows a quantum wire formed using epitaxial growth over a dielectric patterned planar substrate. It is relatively easy to create quantum wells in either of these techniques; however, in order to create quantum wires and dots one still needs e-beam lithography to pattern the grooves and window templates.

Quantum Structure Nanofabrication Using Strain-Induced Self-Assembly

A more recent technique for fabricating quantum wires and dots involves strain-induced self-assembly [7.65, 68]. The term self-assembly represents a process where a strained 2-D system reduces its energy by changing into a 3-D morphology. The material combination most commonly used for this technique is the $In_xGa_{1-x}As/GaAs$ system, which offers a large lattice mismatch (7.2% between InAs and GaAs) [7.69, 70], although Ge dots on Si substrate have recently also attracted considerable attention [7.71]. This method relies on lattice mismatch between an epitaxially grown layer and its substrate, resulting in the formation of an array of quantum dots or wires. Figure 7.49 shows a schematic of the strain-induced self-assembly process. When the lattice constants of the substrate and the epitaxial layer differ markedly, only the first few monolayers deposited crystallize in the form of epitaxially strained layers in which the lattice constants are equal. When a critical thickness is exceeded, significant strain occurs in the layer, leading to the breakdown of this ordered structure and to the spontaneous formation of randomly distributed islets with regular shapes and similar sizes (usually < 30 nm in diameter). This mode of growth is usually referred to as the Stranski–Krastanow mode. The size, separation and height of the quantum dot depend on the deposition parameters (the total amount of deposited material, the growth rate, and the temperature) and material combinations. As can be seen, this is a very convenient method for growing perfect crystalline nanostructures over a large area without any lithography or etching. One major drawback of this technique is the randomness of the quantum dot distribution. It should be mentioned that this technique can also be used to fabricate quantum wires via strain relaxation bunching at the step edges.

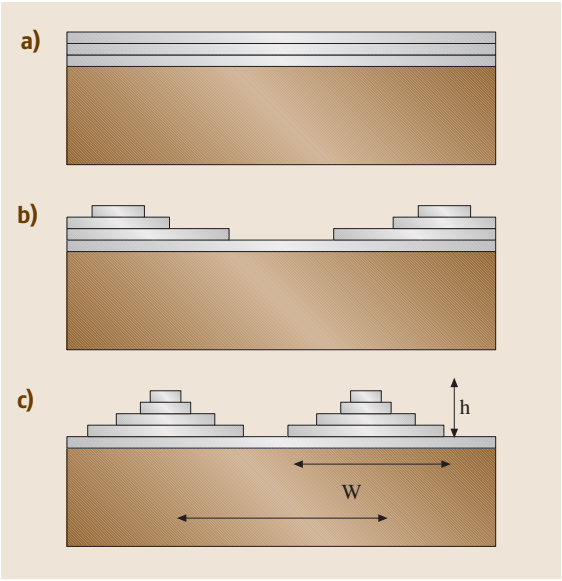


Fig. 7.49a–c Stranski–Krastanow growth mode, **(a)** 2-D wetting layer, **(b)** growth front roughening and break-up, and **(c)** coherent 3-D self-assembly

7.3.3 Scanning Probe Techniques

The invention of scanning probe microscopy (SPM) in the 1980s revolutionized atomic-scale imaging and spectroscopy. In particular, scanning tunneling and atomic force microscopes (STM and AFM) have found widespread application in physics, chemistry, material science, and biology. The ability to perform atomic-scale manipulation, lithography and nanomachining using such probes was considered from the beginning and has matured considerably over the past decade. In this

section, after a brief introduction to scanning probe microscopes, we will discuss several important nanolithography and machining techniques which have been used to create nanometer-sized structures.

Scanning probe microscopy systems involve controlling the movement of an atomically sharp tip in close proximity to or in contact with a surface with subnanometer accuracy. Piezoelectric positioners are typically used in order to achieve such accuracy. High-resolution images can be acquired by raster scanning the tips over a surface while simultaneously monitoring the interaction of the tip with the surface.

In scanning tunneling microscope systems, a bias voltage is applied to the sample and the tip is positioned close enough to the surface for a tunneling current to develop across the gap (Fig. 7.50a). Because this current is extremely sensitive to the distance between the tip and the surface, scanning the tip in the x-y plane while recording the tunnel current permits the surface topography to be mapped with atomic-scale resolution. In a more common mode of operation, the amplified current signal is connected to the z-axis piezoelectric positioner through a feedback loop, so that the current and therefore the distance is kept constant throughout the scanning. In this configuration, the picture of the surface topography is obtained by recording the vertical position of the tip at each x-y position.

The STM system only works for conductive surfaces because of the need to establish a tunneling current. Atomic force microscopy, on the other hand, provides a way to image conducting and nonconducting surfaces. In AFM, the tip is attached to a flexible cantilever and is brought into contact with the surface (Fig. 7.50b). The force between the tip and the surface is detected by sensing the cantilever deflection. A topographic image of the surface is obtained by plotting the deflection as a function of the x-y position. In a more common mode of operation, a feedback loop is used to maintain a constant deflection while the topographic information is obtained from the vertical displacement of the cantilever. Some scanning probe systems use a combination of AFM and STM modes: the tip is mounted in a cantilever with electrical connection so that both the surface force and the tunneling current are controlled or monitored. STM systems can be operated in ultrahigh vacuum (UHV STM) or in air, whereas AFM systems are typically operated in air. When a scanning probe system is operated in air, water adsorbed onto the sample surface accumulates underneath the tip, forming a meniscus between the tip and the surface. This water meniscus plays an important role in some of the scanning probe techniques described below.

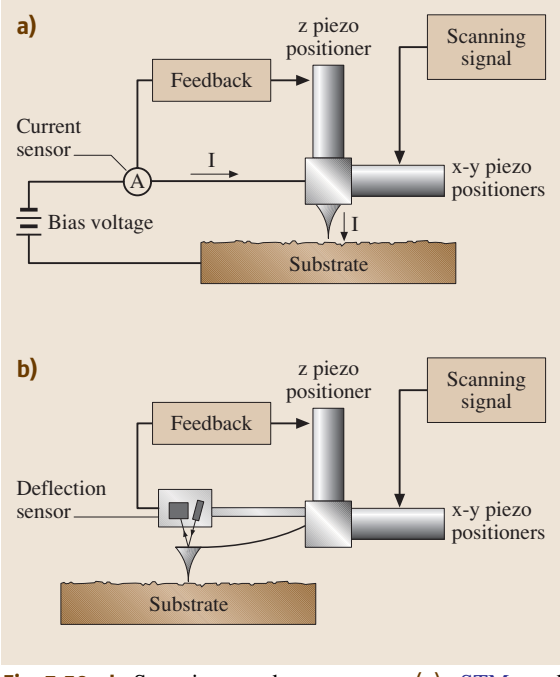


Fig. 7.50a,b Scanning probe systems: **(a)** STM and **(b)** AFM

Scanning Probe–Induced Oxidation

The local nanometer-scale oxidation of various materials can be achieved using scanning probes operated in

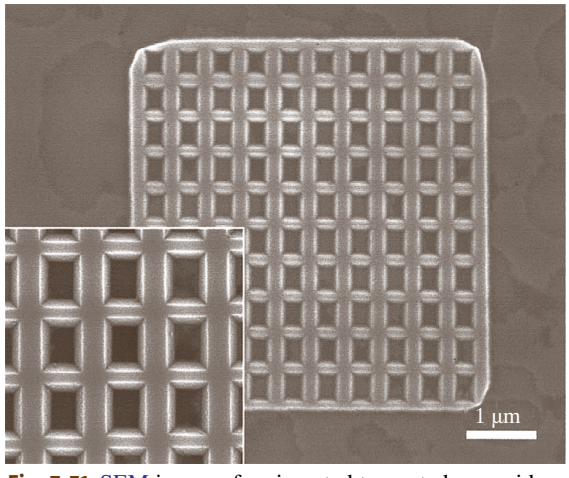


Fig. 7.51 SEM image of an inverted truncated pyramid array fabricated on a silicon SOI wafer by SPM oxidation, and subsequent etch in TMAH (pitch is 500 nm) [7.72]

air and biased at a sufficiently high voltage, Fig. 7.51. Tip biases of −2 to −10 V are normally used, with writing speeds of 0.1–100 μm/s in an ambient humidity of 20%–40%. It is believed that the water meniscus formed at the contact point serves as an electrolyte such that the biased tip anodically oxidizes a small region of the surface [7.73]. The most common application of this principle is the oxidation of hydrogen-passivated silicon. To passivate the surface of the silicon with hydrogen atoms, it is often dipped in HF solution. Patterns of oxide "written" on a silicon surface can be used as a mask for wet or dry etching. Patterns with linewidths of 10 nm have been successfully transferred to a silicon substrate in this fashion [7.74]. Various metals have also been locally anodized (with aluminium or titanium for example) using this approach [7.75]. An interesting variant of this process is the anodization of deposited amorphous silicon [7.76]. Amorphous silicon can be deposited at low temperatures onto a variety of materials. The deposited silicon layer can be patterned and used as, for example, the gate of a 0.1 μm CMOS transistor [7.77], or it can be used as a mask to pattern an underlying film. The major drawback of this technique is poor reproducibility due to tip wear during the anodization. However, the application of AFM performed in noncontact mode has overcome this problem [7.73].

Scanning Probe Resist Exposure and Lithography

Electrons emitted from a biased SPM tip can be used to expose a resist in a similar way to e-beam lithography (Fig. 7.52) [7.77]. Various systems have been used for this lithographic technique, including constant current STM, noncontact AFM and AFM with constant tip–resist force and constant current. The systems that use AFM cantilevers have the advantage that imaging and alignment tasks can be performed without exposing the resist. Resists that are well characterized for e-beam lithography (such as PMMA or SAL601) have been used with scanning probe lithography to achieve reliable sub-100 nm lithography. The procedure for this process is as follows. The wafers are cleaned and the native oxide (for silicon or poly) is removed with a HF dip. A 35–100 nm-thick resist is then spin-coated onto the surface. Exposure is achieved by moving the SPM tip over the surface while applying a bias voltage that is sufficiently high to produce electron emission from the tip (a few tens of volts). The resist is developed in a standard solution following the exposure. Features of less than 50 nm in width have been achieved with this procedure.

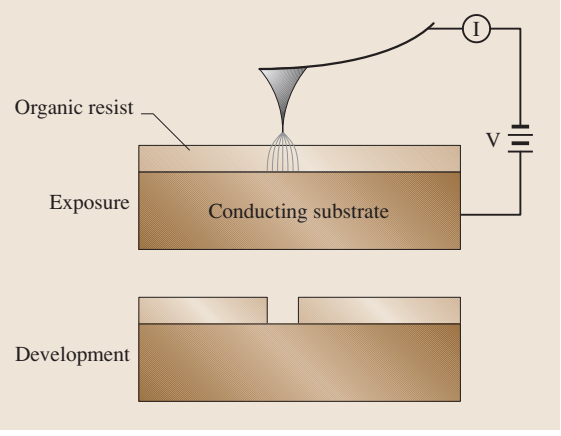


Fig. 7.52 Scanning probe lithography with organic resist

Dip-Pen Nanolithography

In dip-pen nanolithography (DPN), the tip of an AFM operated in air is "inked" with a chemical of interest and brought into contact with a surface. The ink molecules flow from the tip onto the surface, as with a fountain pen. The water meniscus that naturally forms between the tip and the surface enables the diffusion and transport of the molecules, as shown in Fig. 7.53. Inking can be done by dipping the tip in a solution containing a low concentration of the molecules followed by a drying step (blowing dry with compressed difluoroethane for instance). Linewidths down to 12 nm, with a spatial resolution of 5 nm, have been demonstrated with this technique [7.78]. Species patterned with DPN include conducting polymers, gold, dendrimers, DNA, organic dyes, antibodies, and alkanethiols. Alkanethiols have been also used as an organic monolayer mask to etch a gold layer and then etch the exposed silicon substrate. One can also use a heated AFM cantilever to control the deposition of a solid organic ink. This tech-

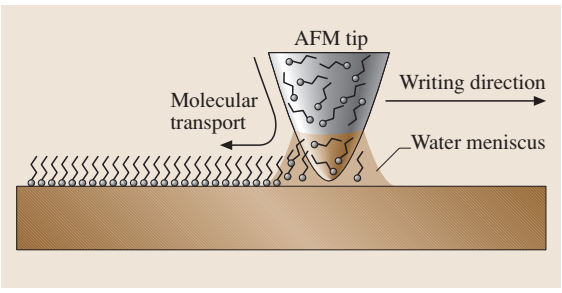


Fig. 7.53 Schematic of the working principles of dip-pen nanolithography

nique was recently reported by *Sheehan* et al. [7.79], where 100 nm lines of octadecylphosphonic acid (melting point: 100 °C) were written using a heated AFM probe [7.79].

Other Scanning Probe Nanofabrication Techniques

A great variety of nanofabrication techniques based on scanning probe systems have been demonstrated. Some of these are proof-of-concept demonstrations and so are yet to be evaluated as viable and repeatable fabrication processes. For example, a substrate can be mechanically machined using STM/AFM tips acting as plows or engraving tools [7.80]. This can be used to directly create structures in the substrate, although it is more commonly used to pattern a resist for a subsequent etch, lift-off or electrodeposition step. Mechanical nanomachining with SPM probes can be facilitated by heating the tip above the glass transition of a polymeric substrate material. This approach has been applied to SPM-based high-density data storage in polycarbonate substrates [7.81].

Electric fields strong enough to induce the emission of atoms from the tip can be easily generated by applying voltage pulses of more than 3 V. This phenomenon has been used to transfer material from the tip to the surface and vice versa. Ten to twenty nanometer mounds of metals such as Au, Ag or Pt have been deposited or removed from a surface in this fashion [7.82]. The same approach has been used to extract single atoms from a semiconductor surface and redeposit them elsewhere [7.83]. The manipulation of nanoparticles, molecules and single atoms on a surface has also been achieved by simply pushing or sliding them with the SPM tip [7.84]. Metals can also be deposited locally by the STM chemical vapor deposition technique [7.85]. In this technique, a precursor organometallic gas is introduced into the STM chamber. A voltage pulse applied between the tip and the surface dissociates the precursor gas into a thin layer of metal. Local electrochemical etching [7.86] and electrodeposition [7.87] are also possible using SPM systems. A droplet of the appropriate solution is first placed on the substrate. Then the STM tip is immersed in the droplet and a voltage is applied. In order to reduce faradaic currents, the tip is coated with wax so that only the very end is exposed to the solution. Sub-100 nm feature sizes have been achieved using this technique.

Using a single tip to serially produce the desired modification in a surface leads to very slow fabrication processes that are impractical for mass production. Many of the scanning probe techniques developed so far, however, could also be performed by an array of tips, which would increase their throughput and make them more competitive with other nanofabrication processes. This approach has been demonstrated for imaging, lithography [7.88] and data storage [7.89] using both one-dimensional and two-dimensional arrays of scanning probes. With the development of larger arrays, with individual advances in force, vertical position and current control, we may see these techniques being used in standard industrial fabrication processes.

7.3.4 Self-Assembly and Template Manufacturing

Self-assembly is a nanofabrication technique that involves aggregation of colloidal nanoparticles into the final desired structure [7.90]. This aggregation can be either spontaneous (entropic) and due to thermodynamic minima (energy minimization) constraints, or chemical and due to the complementary binding of organic molecules and supramolecules (molecular self-assembly) [7.91]. Molecular self-assembly is one of the most important techniques used for the development of complex functional structures in biology. Since these techniques require that the target structures be thermodynamically stable, it tends to produce structures that are relatively defect-free and self-healing. Self-assembly is by no means limited to molecules or the nanodomain, and it can be carried out on just about any scale, making it a powerful bottom-up assembly and manufacturing method (multiscale ordering). Another attractive feature of this technique relates to the possibility of combining self-assembly properties of organic molecules with the electronic, magnetic, and photonic properties of inorganic components. Template manufacturing is another bottom-up technique which utilizes material deposition (electroplating, CVD, and so on) into nanotemplates in order to fabricate nanostructures. The nanotemplates used in this technique are usually prepared using self-assembly techniques. In the following sections, we will discuss various important self-assembly and template manufacturing techniques that are currently being researched extensively.

Physical and Chemical Self-Assembly

The central theme behind the self-assembly process is the spontaneous (physical) or chemical aggregation of colloidal nanoparticles [7.92]. Spontaneous self-assembly exploits the tendency of monodispersed nano- or submicrocolloidal spheres to organize into a face-centered cubic (FCC) lattice. The force driving this process is the desire of the system to achieve a ther-

modynamically stable state (minimum free energy). In addition to spontaneous thermal self-assembly, gravitational, convective and electrohydrodynamic forces can also be used to induce aggregation into complex 3-D structures. Chemical self-assembly requires the attachment of a single molecular organic layer (self-assembled monolayer or SAM) to the colloidal particles (organic or inorganic) and subsequent self-assembly of these components into a complex structures using molecular recognition and binding.

Physical Self-Assembly. This is an entropy-driven method that relies on the spontaneous organization of colloidal particles into a relatively stable structure through noncovalent interactions. For example, colloidal polystyrene spheres can be assembled into a 3-D structure on a substrate that is held vertically in the colloidal solution, Fig. 7.54 [7.93,94]. Upon the evaporation of the solvent, the spheres aggregate into a hexagonal close-packed (HCP) structure. The interstitial pore size and density are determined by the polymer sphere size. The polymer spheres can be etched into smaller sizes after forming the HCP arrays, thereby altering the template pore separations [7.95]. This technique can fabricate large patterned areas in a quick, simple and cost-effective way. A classic example is the natural assembly of on-chip silicon photonic band-gap crystals [7.93] that are capable of reflecting the light arriving in any direction over a certain wavelength range [7.96]. In this method, a thin layer of silica colloidal spheres are assembled on a silicon substrate. This is achieved by placing a silicon wafer vertically in a vial containing an ethanolic suspension of silica spheres. A temperature gradient across the vial aids the flow of silica spheres. Figure 7.55 shows the cross-sectional SEM image of a thin planar opal template assembled directly on a Si wafer from 855 nm spheres. Once such a template is prepared, LPCVD can used to fill the interstitial spaces with Si, so that the high refractive index of silicon provides the necessary bandgap.

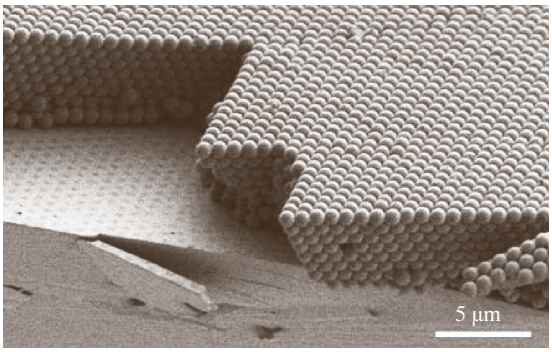


Fig. 7.55 Cross-sectional SEM image of a thin planar opal silica template (spheres are 855 nm in diameter) assembled directly onto a Si wafer [7.93]

One can also deposit colloidal particles into a patterned substrate (template-assisted self-assembly, TASA) [7.97,98]. This method is based on the principle that when an aqueous dispersion of colloidal particles is allowed to dewet from a solid surface that is already patterned, the colloidal particles are trapped by the recessed regions and assembled into aggregates of shapes and sizes determined by the geometric confinement provided by the template. The patterned arrays of templates can be fabricated using conventional contact-mode photolithography which provides control over the shapes and dimensions of the templates, thereby allowing the assembly of complex structures from colloidal particles.

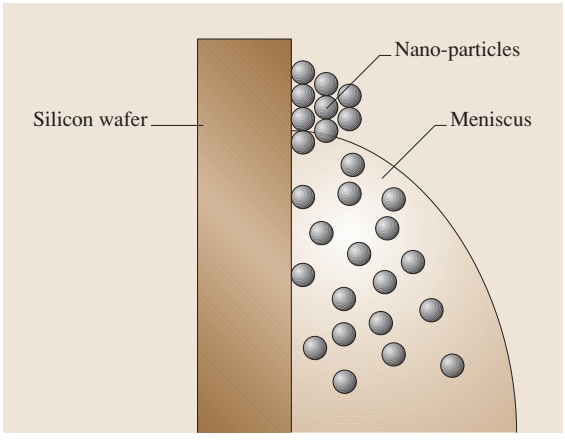


Fig. 7.54 Colloidal particle self-assembly onto solid substrates upon drying in vertical position

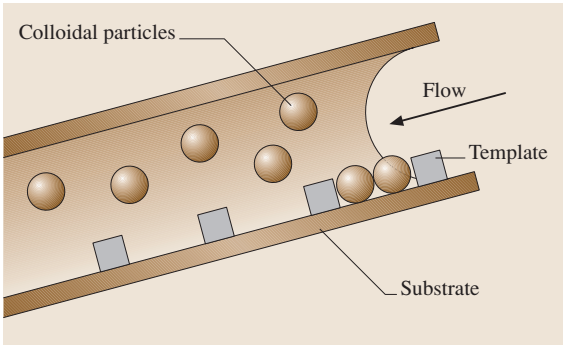


Fig. 7.56 A cross-sectional view of the fluidic cell used for template-assisted self-assembly

A cross-sectional view of a fluidic cell used in TASA is shown in Fig. 7.56. The fluidic cell has two parallel glass substrates to confine the aqueous dispersion of the colloidal particles. The surface of the bottom substrate is patterned with a 2-D array of templates. When the aqueous dispersion is allowed to slowly dewet across the cell, the capillary force exerted on the liquid pushes the colloidal spheres across the surface of the bottom substrate until they are physically trapped by the templates. If the concentration of the colloidal dispersion is high enough, the template will be filled by the maximum number of colloidal particles determined by the geometrical confinement. This method can be used to fabricate a variety of polygonal and polyhedral aggregates that are otherwise difficult to generate [7.99].

Chemical Self-Assembly. Organic and supramolecular SAMs play a critical role in colloidal particle self-assembly. SAMs are robust organic molecules that are chemically adsorbed onto solid substrates [7.100]. They often have a hydrophilic (polar) head which can be bonded to various solid surfaces and a long hydrophobic (nonpolar) tail which extends outward. SAMs are formed by the immersion of a substrate in a dilute solution of the molecule in an organic solvent. The resulting film is a dense organization of molecules arranged to expose the end group. The durability of the SAM is highly dependent on the strength of the anchoring to the surface of the substrate. SAMs have been widely studied because the end group can be functionalized to form precisely arranged molecular arrays for various applications ranging from simple, ultrathin insulators and lubricants to complex biological sensors. Chemical self-assembly uses organic or supramolecular SAMs as the binding and recognition sites for fabricating complex 3-D structures from colloidal nanoparticles. The most commonly used organic monolayers include: 1) organosilicon compounds on glass and native surface oxide layers of silicon, 2) alkanethiols, dialkyl disulfides and dialkyl sulfides on gold, 3) fatty acids on alumina and other metal oxides, and 4) DNA.

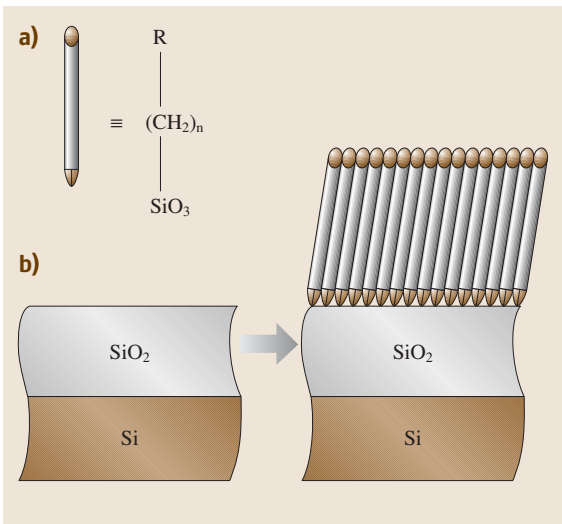


Fig. 7.57 **(a)** Alkylsiloxane formed from the adsorption of alkyltrichlorosilane onto Si/SiO_2 substrates. **(b)** Schematic representation of the process

Octadecyltrichlorosilane (OTS) is the most common organosilane used in the formation of SAMs mainly due to the fact that it is simple, readily available and forms good, dense layers [7.101, 102]. Alkyltrichlorosilane monolayers can be prepared on clean silicon wafers with SiO_2 on the surface (with almost 5×10^{14} SiOH groups/cm^2). Figure 7.57 shows a schematic representation of the formation of alkylsiloxane monolayers by the adsorption of alkyltrichlorosilanes from solution onto Si/SiO_2 substrates. Since the silicon–chlorine bond is susceptible to hydrolysis, the amount of water in the system must be limited in order to obtain good quality monolayers. Monolayers made of methyl- and vinyl-terminated alkylsilanes are autophobic to the hydrocarbon solution and hence emerge uniformly dry from the solution, whereas monolayers made of ester-terminated alkylsilanes emerge wet from the solution used in their formation. The disadvantage of this method is that a cloudy film is deposited on the surface (due to formation of a gel of polymeric siloxane) if the alkyltrichlorosilane in the solvent adhering to the substrate is exposed to water.

Alkanethiols ($X(CH_2)_nSH$, where X is the end-group) on gold form another important group of organic SAM systems [7.100, 103–105]. A major advantage of using gold as the substrate material is that it does not have a stable oxide and so it can be handled in ambient conditions. When a fresh, clean, hydrophilic gold substrate is immersed (for several minutes to several hours) in a dilute solution (10^{-3} M) of the organic sulfur compound (alkanethiols) in an inorganic solvent, close-packed, oriented monolayers can be obtained. Sulfur is used as the head group because of the strong interaction with gold substrate (44 kcal/mol), resulting in the formation of a close-packed, ordered monolayer. The end-group of the alkanethiol can be modified to give hydrophobic or hydrophilic properties to the adsorbed layer. Another method for depositing alkanethiol SAM is soft lithography. This technique is based on ink-

ing a PDMS stamp with alkanethiol and its subsequent transfer to planar and nonplanar substrates. Alkanethiol-functionalized surfaces (planar, nonplanar, spherical) can also be used to self-assemble a variety of intricate 3-D structures [7.106].

Carboxylic acid derivatives self-assemble on surfaces (such as glass, Al_2O_3 and Ag_2O) through an acid-base reaction, giving rise to monolayers of fatty acids [7.107]. The time required for the formation of a complete monolayer increases with decreased concentration. Higher concentrations of the carboxylic acid are required to form a monolayer on gold than on Al_2O_3. This is due to the different affinities of the COOH group to these substances (more affinity to Al_2O_3 and glass than to gold) and also the surface concentrations of the salt-forming oxides in the two substrates. In the case of amorphous metal oxide surfaces, the chemisorption of alkanoic acids is not unique. For example, on Ag_2O, the two carboxylate oxygen atoms bind to the substrate in an almost symmetrical manner, resulting in ordered monolayers with a chain tilt angle from the surface normal of 15° to 25°. However, on CuO and Al_2O_3, the oxygen atoms bind themselves symmetrically and the chain tilt angle is close to 0°. The structure of the monolayers is thus the result of a balance between the various interactions taking place in the polymer chains.

Deoxyribonucleic acid (DNA) – the framework on which all life is built – can be used to self-assemble nanomaterials into useful macroscopic aggregates that display a number of desired physical properties [7.108]. DNA consists of two strands that are coiled around each other to form a double helix. Singular strands of nucleotides are left when the two strands are uncoiled . These nucleotides consist of a sugar (a pentose ring), a phosphate (PO_4) and a nitrogenous base. The correct order and architecture of these components is essential to achieving the proper structure of a nucleotide. Four nucleotides are typically found in DNA, adenine (A), guanine (G), cytosine (C), and thymine (T). A key property of the DNA structure is that the nucleotides described bind specifically to another nucleotide when arranged in the two-strand double helix (A to T, and C to G). This specific bonding capability can be used to assemble nanophase material and nanostructures [7.109]. For example, nucleotide-functionalized nanogold particles have been assembled into complex 3-D structures by attaching DNA strands to the gold via an enabler or linker [7.110]. In separate work, DNA was used to assemble nanoparticles into macroscopic materials. This method uses alkane dithiol as the linker molecule to connect the DNA template to the nanoparticle. The thiol groups at each end of the linker molecule covalently attach themselves to the colloidal particles to form aggregate structures [7.111].

Template Manufacturing

Template manufacturing refers to a set of techniques that can be used to fabricate organic or inorganic 3-D structures from a nanotemplate. These templates differ in material, pattern, feature size, overall template size and periodicity. Although nanotemplates can be fabricated using e-beam lithography, the serial nature of this technique prohibits its widespread application. Self-assembly is the preferred technique since it can produce large-area nanotemplates in a massively parallel fashion. Several nanotemplates have been investigated for use in template manufacturing. These include polymer colloidal spheres, alumina membranes, and nuclear track-etched membranes. Colloidal spheres can be deposited in a regular 3-D array using the techniques described in the previous section (see Figs. 7.54–7.56). Porous aluminium oxide membranes can be fabricated by the anodic oxidation of aluminium [7.112]. The oxidized film consists of columnar arrays of hexagonal close-packed pores separated at distances comparable to the pore size. By controlling the electrolyte species, temperature, anodizing voltage and time, different pore sizes, densities and heights can be obtained. The pore size and depth can also be adjusted by etching the oxide in an appropriate acid. Templates of porous polycarbonate or mica membranes can be fabricated by nuclear track-etched membranes [7.113]. This technique is based on the passage of high-energy decay fragments from a radioactive source through a dielectric material. The particles leave behind chemically active damaged tracks which can then be etched to create pores throughout the thickness of the membrane [7.114, 115]. Unlike the other methods, the pore separation and hence the pore density is independent of the pore size. The pore density is only determined by the irradiation process.

Subsequent to template fabrication, the interstitial spaces (in the case of colloidal spheres) or pores (for alumina and polycarbonate membranes) in the template are filled with the desired material [7.95, 116]. This can be achieved using a variety of deposition techniques, such as electroplating and CVD. The final structure can be a composite of nanotemplate and deposited material, or the template can be selectively etched resulting in an air-filled 3-D complex structure. For example, nickel [7.117], iron [7.118] and cobalt [7.119] nanowires have been electrochemically grown in porous template matrices. Three-dimensional photonic crystals

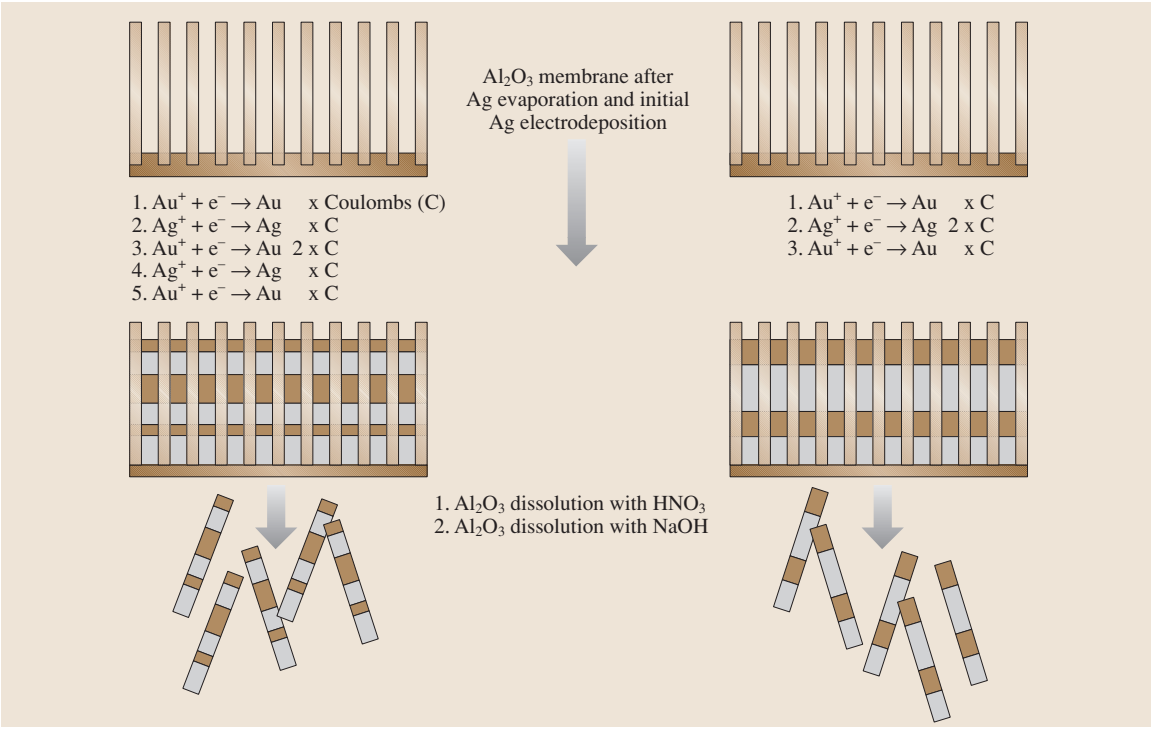


Fig. 7.58 Synthesis of nanobarcode particles

have been fabricated by the electrochemical deposition of CdSe and silicon into polystyrene and silica colloidal assembly templates [7.93, 120]. An interesting example of template-assisted manufacturing is the synthesis of nanometer-sized metallic barcodes [7.121]. These nanobarcodes are prepared by the electrochemical reduction of metallic ions into the pores of an aluminium oxide membrane followed by their release through the etching of the template [7.122–124]. This procedure is schematically illustrated in Fig. 7.58. A back-side silver film is used as the working electrode for the reduction of metallic ions (silver and gold in this case) from solution. Up to seven different metallic segments as short as 10 nm and as long as several micrometers, with 13 distinguishable stripes, have been fabricated using this technique. Optical reflectivity is used to read out the stripe pattern encoded in the metal particles [7.121]. Figure 7.59 shows optical and field emission scanning electron microscope images of a Au-Ag multistripe nanobarcode

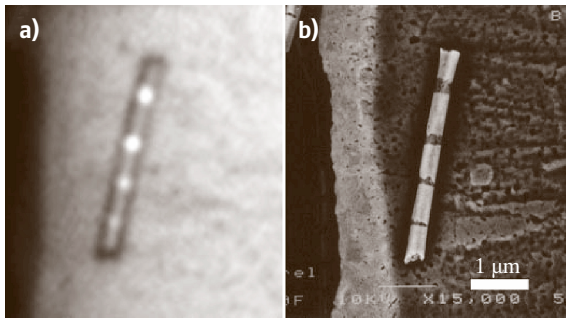


Fig. 7.59 (**a**) Optical and (**b**) FE-SEM images of Au-Ag multistripe particles [7.121]

(Ag stripes ranging in length from 60 to 240 nm separated by Au segments of 550 nm can be seen). These coded nanoparticles can be used in fluorescence and mass spectrometry-based assays, enabling a wide variety of bioanalytical measurements to be taken.

7.4 Summary and Conclusions

In this chapter, we have discussed various micro/nanofabrication techniques used to manufacture structures covering a wide range of dimensions (mm–nm). Starting with some of the most common microfabrication techniques (lithography, deposition and etching), we presented an array of micromachining and MEMS technologies that can be used to fabricate microstructures down to $\approx 1\,\mu m$. These techniques have attained an adequate level of maturity to allow for a variety of MEMS-based commercial products (pressure sensors, accelerometers, gyroscopes, and so on). More recently, nanometer-sized structures have attracted an enormous amount of interest. This is mainly due to their unique electrical, magnetic, optical, thermal and mechanical properties. These could lead to a variety of electronic, photonic and sensing devices with superior performance compared to their macro counterparts. Subsequent to our discussion on MEMS and micromachining, we presented several important nanofabrication techniques currently under intense investigation. Although e-beam and other high-resolution lithographies can be used to fabricate nanometer-size structures, their serial nature and/or cost preclude their widespread application. This has forced investigators to explore alternative and potentially superior techniques such as strain engineering, self-assembly, and nanoimprint lithography. Among these, self-assembly is the most promising method, due to its low cost and its ability to produce nanostructures at different length scales.

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